CM6632A

USB 2.0 High-Definition Audio Processor

DESCRIPTION

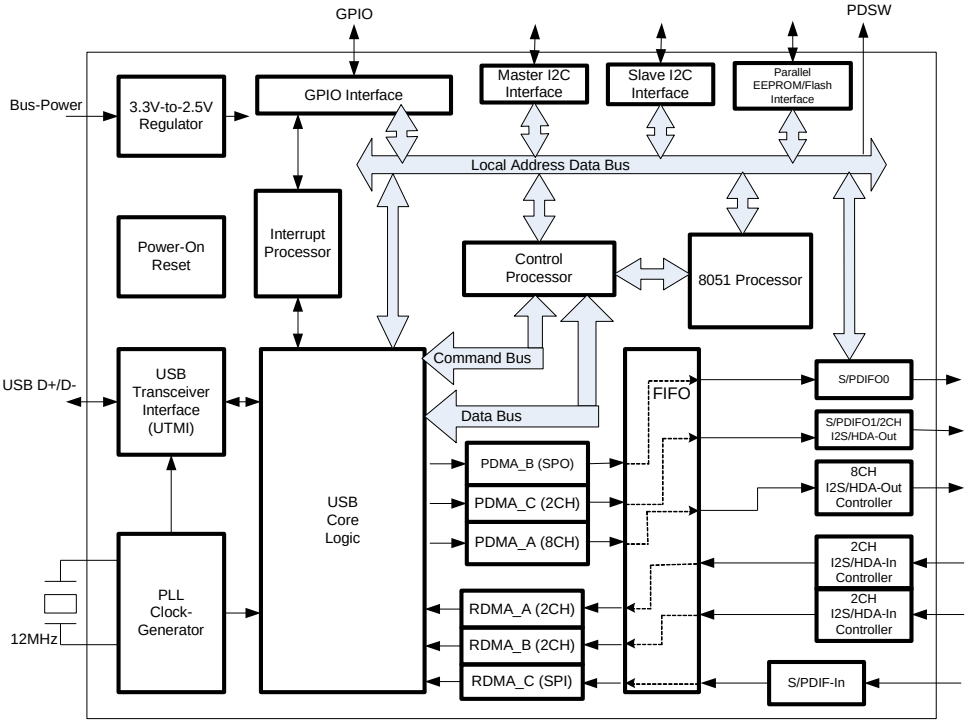
The CM6632A is a USB 2.0 high-speed audio processor that supports the latest USB Audio Device Class V2.0 and high-definition audio processing applications. The CM6632A provides industry-standard HDA and I2S I/O interfaces, supports a maximum of 10 channels of output and 4 channels of input, and also integrates a 192KHz/24-bit S/PDIF transmitter and receiver, making it very versatile.

Furthermore, the CM6632A has an embedded 8051 microprocessor that can enhance the flexibility and functionality with external upgradeable ROM codes. The CM6632A is the most powerful audio core for your high-value USB2.0 audio products.
CM6632A is also capable to support DSD bit stream output. It's a lossless SACD playback technique in PC/Notebook.

FEATURES

- USB specification 2.0 high speed-compatible
- USB audio device class 2.0/1.0-compatible
- USB human interface device (HID) class 1.1-compliant
- Support PCM and DSD bit stream output
- Supports USB suspend/resume/reset functions
- Supports control/interrupt/bulk/isochronous data transfers
- Five pairs of I2S or left-justified serial audio output interfaces (8+2-ch out)
- Two pairs of I2S or left-justified serial audio input interfaces (2+2-ch in)
- I2S input/output support (44.1K/48K/88.2K/ 96K/176.4K/192KHz and 16/24/32 bits
- SPDIF input/output supports up to 192KHz/24-bit transfer rate

BLOCK DIAGRAM



Release Notes

Revision	Date	Description
0.1	2012/08/10	First release of preliminary technical information
0.2	2012/10/18	-Add DSD support
1.0	2012/10/23	Formal release
1.1	2012/12/20	Modify software features

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1 Description and Overview

The CM6632A is a high-speed USB 2.0 high-speed audio processor that supports the latest USB Audio Device Class V2.0 and high-definition audio processing applications. The CM6632A provides industry-standard HDA and I2S I/O interfaces, supports a maximum of 10 channels of output and 4 channels of input, and also integrates a 192KHz/24-bit S/PDIF transmitter and receiver, making it very versatile. Furthermore, the CM6632A has an embedded 8051 microprocessor that can enhance the flexibility and functionality with external upgradeable ROM codes. The CM6632A is the most powerful audio core for your high-value USB2.0 audio products.

2 Features

USB Compliance

- USB specification 2.0 high-speed-compatible
- Latest USB audio device class 2.0/1.0-compatible
- USB human interface device (HID) Class 1.1-compliant
- Supports USB suspend/resume/reset functions
- Asynchronous synchronization transfer to reduce clock jitter
- Supports control/interrupt/bulk/isochronous data transfers

Audio Engine

- 3 Independent playback streams:
  - Supported sample rate: 44.1K/48K/88.2K/96K/176.4K/192KHz (192K/176.4KHz are available only in USB Audio Class 2.0/High-speed mode)
  - Supported bit length: 16/24/32-bit
  - PDMA#A supports max. 8-ch to I2S output
  - PDMA#B supports S/PDIF output
  - PDMA#C supports 2-ch to I2S output
- 3 Independent capture streams:
  - Supported sample rate: 44.1K/48K/88.2K/96K/176.4K/192KHz (192K/176.4KHz are available only in USB Audio Class 2.0/High-speed mode)
  - Supported bit length: 16/24/32-bit
  - RDMA#A supports 2-ch from I2S input
  - RDMA#B supports 2-ch from I2S input
  - RDMA#C supports S/PDIF input (192KHz receiving supports only Crystal and PLL clock sources)

Audio I/O

- Five pairs of I2S or left-justified serial audio output interfaces (8+2-ch out)
- Two pairs of I2S or left-justified serial audio input interfaces (2+2-ch in)
- All the I2S input/out interfaces support master/slave mode
- Built-in 192K/176.4K/96K/88.2K/48K/44.1KHz, and 16/24-bit S/PDIF transmitter
- Integrated 192K/176.4K/96K/88.2K/48K/44.1KHz, and 16/24-bit S/PDIF receiver
- Supports S/PDIF IN-to-OUT loop-back path for signal transforming between TOSLINK and RCA connections

Integrated 8051 Micro-processor

- Embedded 8051 micro-processor handles comment/protocol transactions
- Connects to an external parallel Flash/EEPROM memory (64kb, 55ns access time is required) for firmware ROM codes
- HID interrupts can be implemented via firmware codes
- Provides maximum HW configuration flexibility with a firmware code upgrade
- VID/PID/product string can be customized via firmware code programming

Control Interface

- Master I2C control interface for external audio devices or EEPROM access
- Slave I2C control interface for external MCU communication
- 9 GPIO pins and 6 GPI pins

General

- Embedded USB 2.0 transceiver (up to 480MB bandwidth)
- Auto detection for high-speed/full-speed
- GPIO pin for USB Audio Class 2.0 and 1.0 application mode configurations
- Single 12MHz crystal input is required (embedded PLL function), or optional oscillator inputs for 49.152 or 24.576MHz (for x48KHz) and 45.158 or 22.5792MHz (for x44.1KHz)
- Single 3.3V power supply (embedded 3.3V to 2.5V regulator for digital core)
- 3.3V digital I/O pads with 5V tolerance
- Industry-standard LQFP-100 package (16 x 16mm)

Optional Value-added Software Features:

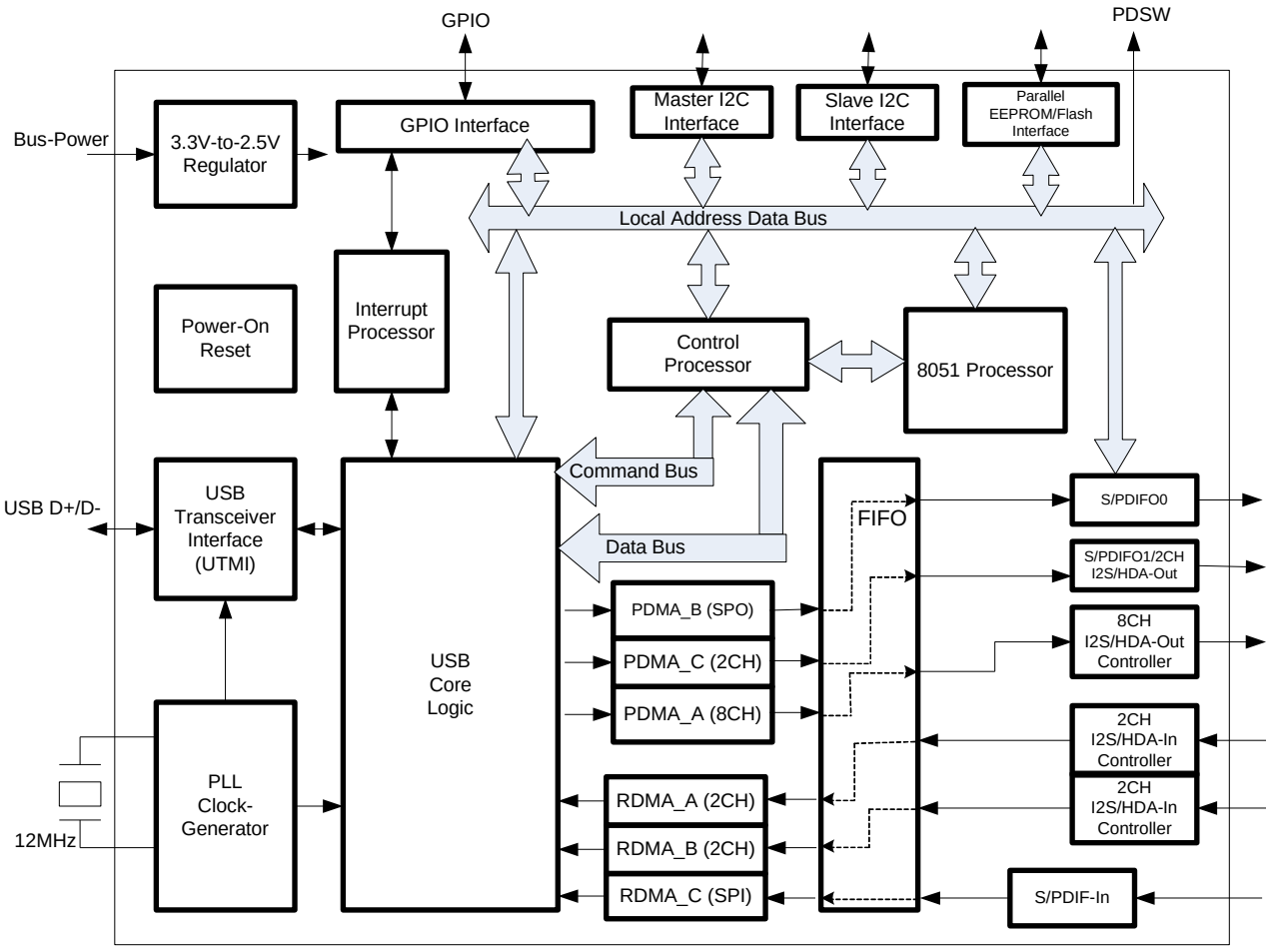
- Cmedia vendor drivers supports USB Audio Class 2.0 and high-speed mode on Windows® XP, Windows® Vista, Windows® 7, Windows® 8 and Mac OS X 10.5.7 (or later) with Cmedia vendor drivers
- USB audio class 1.0 with full-speed/high-speed modes compatible with the Windows® XP, Windows® Vista, Windows® 7 and Windows® 8 UAA driver, Mac OS X and Linux embedded USB audio drivers
- For Windows, Cmedia drivers provide the following key features:
  - Playback feedback endpoints to control data transmission accuracy and maximize audio quality
  - Xear™ Pro
    - Support ASIO2.2 driver

3 Applications

- Multi-channel audio boxes
- Professional audio-PC musician applications (recording mixer, I/O interface, DJ console, keyboard, electric guitar, etc.)
- Laptop docking system with USB 2.0 high-definition audio features
- High-quality USB 2.0 multi-channel headphone/headset
- Portable high-quality USB 2.0 multi-channel sound stations
- USB A/V receiver
- ExpressCard-compatible USB 2.0 audio adaptor for laptops
- Wired or wireless USB hub with audio features

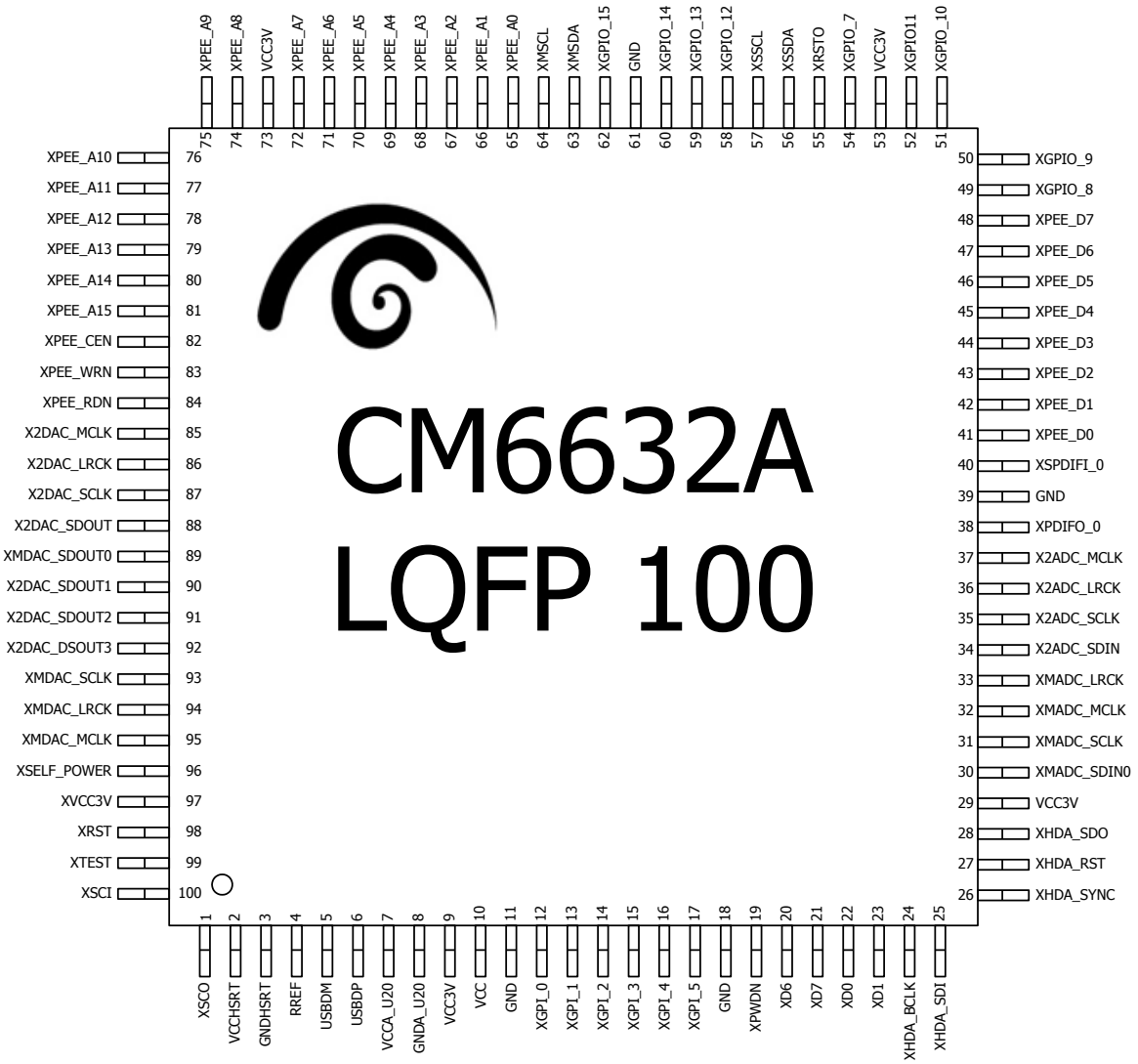
4 Block Diagram

CM6632A Functional Block Diagram



5 Pin Assignment

5.1 Pin-Out Diagram



5.2 Pin Description

Pin #	Symbol	I/O	Description
Clock			
1	XSCO	AO	12MHz crystal oscillator output
100	XSCI	AI	12MHz crystal oscillator input
20	XD6	DIO	49.152Mhz oscillator input(for 48, 96,192KHz)
21	XD7	DIO	45.158Mhz oscillator input(for 44.1KHz)
USB 2.0 Bus Interface			
5	USBDM	AIO	USB 2.0 data negative (USB D- signal)
6	USBDP	AIO	USB 2.0 data positive (USB D+ signal)
Power/Ground			
2	VCCHSRT	AI	USB PHY analog power supply pin (3.3V)
3	GNDHSRT	AI	USB PHY analog ground
7	VCCA_U20	AI	USB PHY analog power supply pin (3.3V)
8	GNDA_U20	A	USB PHY analog ground
9	VCC3V	DI	Digital power supply pin (3.3V)
10	VCC	DO	Digital power filter pin (2.5V), connecting external filter capacitors
11	GND	D	Digital ground
18	GND	D	Digital ground
29	VCC3V	DI	Digital power supply pin (3.3V)
39	GND	D	Digital ground
53	VCC3V	DI	Digital power supply pin (3.3V)
61	GND	D	Digital ground
73	VCC3V	DI	Digital power supply pin (3.3V)
97	VCC3V	DI	Digital power supply pin (3.3V)
2-channel I2S ADC_1 Interface (RDMA_A)			
30	XMADC_SDIN0	DI	I2S serial data input for channel 0, 1 Programmable 3.3V input buffer, Schmitt trigger, pull-down
31	XMADC_SCLK	DIO	I2S bit clock Programmable 3.3V bidirectional buffer, pull-down
32	XMADC_MCLK	DO	I2S master clock Programmable 3.3V output buffer
33	XMADC_LRCK	DIO	I2S left/right clock Programmable 3.3V bidirectional buffer, pull-down
2-channel I2S ADC_2 Interface (RDMA_C)			
34	X2ADC_SDIN	DI	I2S serial data input for channel 0, 1 Programmable 3.3V input buffer, Schmitt trigger, pull-down
35	X2ADC_SCLK	DIO	I2S bit clock Programmable 3.3V bidirectional buffer, pull-down

36	X2ADC_LRCK	DIO	I2S left/right clock Programmable 3.3V bidirectional buffer, pull-down
37	X2ADC_MCLK	DO	I2S master clock Programmable 3.3V output buffer
S/PDIF I/O			
38	XSPDIFO_0	DO	S/PDIF transmitter Programmable 3.3V output buffer
40	XSPDIFI_0	DI	S/PDIF receiver 3.3v input buffer, Schmitt trigger, pull-down
Parallel EEPROM/Flash Memory Interface			
41	XPEE_D0	DIO	Parallel EEPROM/FLASH data in/out 0 Programmable 3.3V bidirectional buffer, pull-down
42	XPEE_D1	DIO	Parallel EEPROM/FLASH data in/out 1 Programmable 3.3V bidirectional buffer, pull-down
43	XPEE_D2	DIO	Parallel EEPROM/FLASH data in/out 2 Programmable 3.3V bidirectional buffer, pull-down
44	XPEE_D3	DIO	Parallel EEPROM/FLASH data in/out 3 Programmable 3.3V bidirectional buffer, pull-down
45	XPEE_D4	DIO	Parallel EEPROM/FLASH data in/out 4 Programmable 3.3V bidirectional buffer, pull-down
46	XPEE_D5	DIO	Parallel EEPROM/FLASH data in/out 5 Programmable 3.3V bidirectional buffer, pull-down
47	XPEE_D6	DIO	Parallel EEPROM/FLASH data in/out 6 Programmable 3.3V bidirectional buffer, pull-down
48	XPEE_D7	DIO	Parallel EEPROM/FLASH data in/out 7 Programmable 3.3V bidirectional buffer, pull-down
82	XPEE_CEN	DO	Parallel EEPROM/FLASH chip enable, active low Programmable 3.3V output buffer
83	XPEE_WRN	DIO	Parallel EEPROM/FLASH write enable, active low Programmable 3.3V bidirectional buffer, pull-down
84	XPEE_RDN	DIO	Parallel EEPROM/FLASH read enable, active low Programmable 3.3V bidirectional buffer, pull-down
65	XPEE_A0	DIO	Parallel EEPROM/FLASH address 0 Programmable 3.3V bidirectional buffer, pull-down
66	XPEE_A1	DIO	Parallel EEPROM/FLASH address 1 Programmable 3.3V bidirectional buffer, pull-down
67	XPEE_A2	DIO	Parallel EEPROM/FLASH address 2 Programmable 3.3V bidirectional buffer, pull-down
68	XPEE_A3	DIO	Parallel EEPROM/FLASH address 3 Programmable 3.3V bidirectional buffer, pull-down
69	XPEE_A4	DIO	Parallel EEPROM/FLASH address 4 Programmable 3.3V bidirectional buffer, pull-down
70	XPEE_A5	DIO	Parallel EEPROM/FLASH address 5 Programmable 3.3V bidirectional buffer, pull-down
71	XPEE_A6	DIO	Parallel EEPROM/FLASH address 6 Programmable 3.3V bidirectional buffer, pull-down
72	XPEE_A7	DIO	Parallel EEPROM/FLASH address 7 Programmable 3.3V bidirectional buffer, pull-down
74	XPEE_A8	DIO	Parallel EEPROM/FLASH address 8 Programmable 3.3V bidirectional buffer, pull-down
75	XPEE_A9	DIO	Parallel EEPROM/FLASH address 9 Programmable 3.3V bidirectional buffer, pull-down
76	XPEE_A10	DIO	Parallel EEPROM/FLASH address 10 Programmable 3.3V bidirectional buffer, pull-down
77	XPEE_A11	DIO	Parallel EEPROM/FLASH address 11 Programmable 3.3V bidirectional buffer, pull-down
78	XPEE_A12	DIO	Parallel EEPROM/FLASH address 12 Programmable 3.3V bidirectional buffer, pull-down
79	XPEE_A13	DIO	Parallel EEPROM/FLASH address 13 Programmable 3.3V bidirectional buffer, pull-down

80	XPEE_A14	DIO	Parallel EEPROM/FLASH address 14 Programmable 3.3V bidirectional buffer, pull-down
81	XPEE_A15	DIO	Parallel EEPROM/FLASH address 15 Programmable 3.3V bidirectional buffer, pull-down
GPI			
12	XGPI_0	DIO	General purpose input 0 Programmable 3.3V input buffer, Schmitt trigger, pull-down
13	XGPI_1	DIO	General purpose input 1 Programmable 3.3V input buffer, Schmitt trigger, pull-down
14	XGPI_2	DIO	General purpose input 2 Programmable 3.3V input buffer, Schmitt trigger, pull-down
15	XGPI_3	DIO	General purpose input 3 Programmable 3.3V input buffer, Schmitt trigger, pull-down
16	XGPI_4	DIO	General purpose input 4 Programmable 3.3V input buffer, Schmitt trigger, pull-down
17	XGPI_5	DIO	General purpose input 5 Programmable 3.3V input buffer, Schmitt trigger, pull-down
GPIO			
54	XGPIO_7	DIO	General purpose input/output 0 (default output). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
49	XGPIO_8	DIO	General purpose input/output 1 (default output). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
50	XGPIO_9	DIO	General purpose input/output 2 (default output). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
51	XGPIO_10	DIO	General purpose input/output 3 (default input). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
52	XGPIO_11	DIO	General purpose input/output 4 (default input). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
58	XGPIO_12	DIO	General purpose input/output 5 (default input). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
59	XGPIO_13	DIO	General purpose input/output 6 (default input). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
60	XGPIO_14	DIO	General purpose input/output 6 (default input). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
62	XGPIO_15	DIO	General purpose input/output 6 (default input). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
MIDI Interface			
22	XD0	DIO	MIDI RXD, serial input port Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
23	XD1	DIO	MIDI TXD, serial output port Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
High-Definition Audio Interface			
24	XHDA_BCLK	DO	HDA link bit clock (24MHz) Programmable 3.3V output buffer
25	XHDA_SDI	DI	HDA link serial data in Programmable 3.3V bidirectional buffer, pull-down
26	XHDA_SYNC	DO	HDA link frame synchronization Programmable 3.3V output buffer
27	XHDA_RST	DO	HDA link reset signal, active low Programmable 3.3V output buffer
28	XHDA_SDO	DO	HDA link serial data out Programmable 3.3V output buffer
2-channel I2S DAC_2 Interface (PDMA_C)			
85	X2DAC_MCLK	DO	I2S master clock Programmable 3.3V output buffer
86	X2DAC_LRCK	DIO	I2S left/right clock Programmable 3.3V bidirectional buffer, pull-down
87	X2DAC_SCLK	DIO	I2S bit clock Programmable 3.3V bidirectional buffer, pull-down

88	X2DAC_SDOUT	DO	I2S serial data output for channel 0, 1 Programmable 3.3V output buffer
8-channel I2S or 2-channel DSD DAC_1 Interface (PDMA_A)			
89	XMDAC_SDOUT0 / DSD left channel	DO	I2S serial data output for channel 0, 1/DSD left channel data Programmable 3.3V output buffer
90	XMDAC_SDOUT1 / DSD right channel	DO	I2S serial data output for channel 2, 3/DSD right channel data Programmable 3.3V output buffer
91	XMDAC_SDOUT2	DO	I2S serial data output for channel 4, 5 Programmable 3.3V output buffer
92	XMDAC_SDOUT3	DO	I2S serial data output for channel 6, 7 Programmable 3.3V output buffer
93	XMDAC_SCLK / DSD SCLK	DIO	I2S bit clock/DSD Serial clock Programmable 3.3V bidirectional buffer, pull-down
94	XMDAC_LRCK	DIO	I2S left/right clock Programmable 3.3V bidirectional buffer, pull-down
95	XMDAC_MCLK	DO	I2S master clock Programmable 3.3V output buffer
2-Wire Master Serial Bus (I2C)			
63	XMSDA	DIO	2-wire master serial data Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
64	XMSCL	DIO	2-wire master serial clock Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
2-Wire Slave Serial Bus (I2C)			
56	XSSDA	DIO	2-wire slave serial data Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
57	XSSCL	DIO	2-wire slave serial clock Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
Miscellaneous			
4	RREF	AI	Connect external reference resistor (12KΩ±1%)
19	XPWDN	DO	External device power down control signal (default tri-state) Programmable 3.3V/5V tolerance output buffer
55	XRSTO	DO	External codec reset (default tri-state) Programmable 3.3V/5V tolerance output buffer
96	XSEL_PWR	DI	Self Power used, 1:self power, 0:bus power Programmable 3.3V input buffer, Schmitt trigger, Pull-down
98	XRST	DI	CM6632A chip reset
99	XTEST	DI	Test mode select pin: H: Test Mode L: Normal Operation

6 Electrical Characteristics

6.1 Maximum Ratings

Test conditions; V_{DD} = 3.3V, DGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Storage temperature	-	-55	-	150	oC
Operating ambient temperature	-	0	25	75	oC
DC supply voltage	-	3.0	3.3	3.6	V
I/O pin voltage	-	GND	-	VDD	V
Power dissipation	-	-	0.15	-	W

6.2 Recommended Operation Conditions

Test conditions: VDD = 3.3V, DGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Input voltage range	-	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage range	-	0	-	V_{DD}	V

6.3 Power Consumption

Test conditions: DVDD = 3.3V, DGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Supply current : power up	-	-	79.42	-	mA
Supply current : power down	-	-	0.163	-	uA

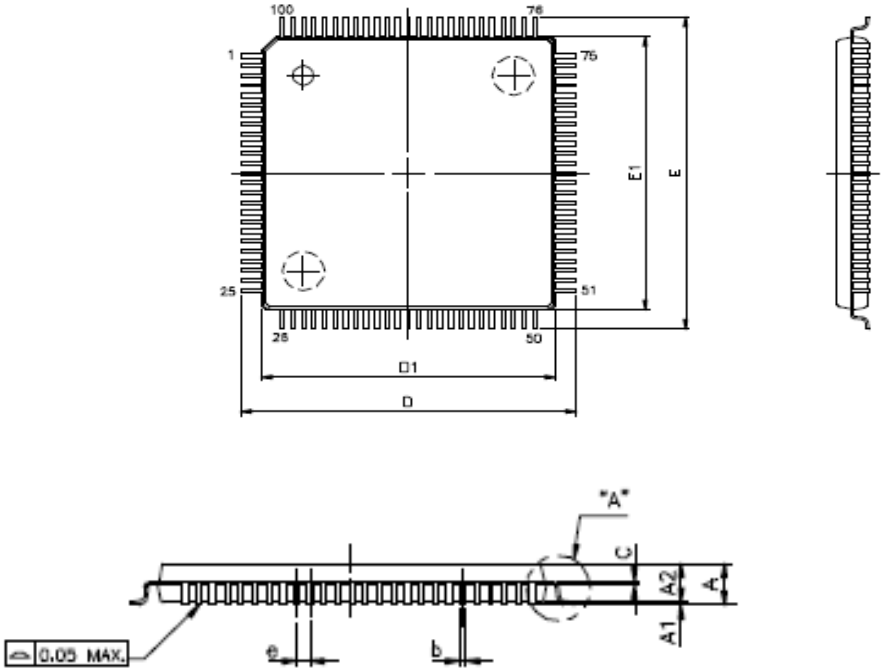
6.4 DC Characteristics

Test Conditions: DVDD = 3.3V, DGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Input voltage range	Vin	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage range	Vout	0	-	V_{DD}	V
High level input voltage	Vih	0.7V_{DD}	-	-	V
Low level input voltage	Vil	-	-	0.3V_{DD}	V
High level output voitage	Voh	2.4	-	-	V
Low level output voltage	Vol		-	0.4	V
Input leakage current	Iil	-10	-	10	uA
Output leakage current	Iol	-10	-	10	uA
Output buffer driver current	-	-	8	-	mA
SPDIF transmit output driver current	-	-	8	-	mA

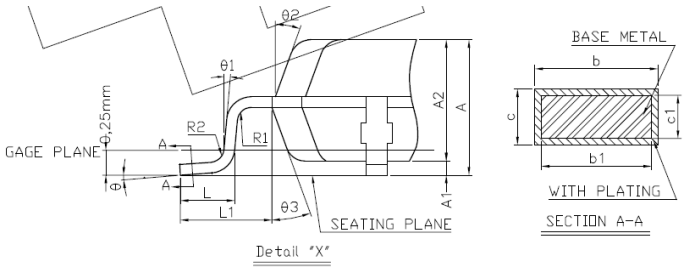
7 Package Dimensions

LQFP-100 (16 x 16mm)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		



NOTES:
1.REFER TO JEDEC MS-026/BCE
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

—End of Datasheet—

C-MEDIA ELECTRONICS INC.

6F., 100, Sec. 4, Civil Boulevard, Taipei, Taiwan 106 R.O.C.

TEL：+886-2-8773-1100

FAX：+886-2-8773-2211

E-MAIL：sales@cmedia.com.tw