DESCRIPTION

The CM6571 is a USB 2.0 audio chip with a built-in 8051 and DSP designed for a wide range of applications. With an internal two-channel ADC/DAC, S/PDIF, it is perfectly suited for gaming headset, speakerphone, surround speaker or Apple docking applications.

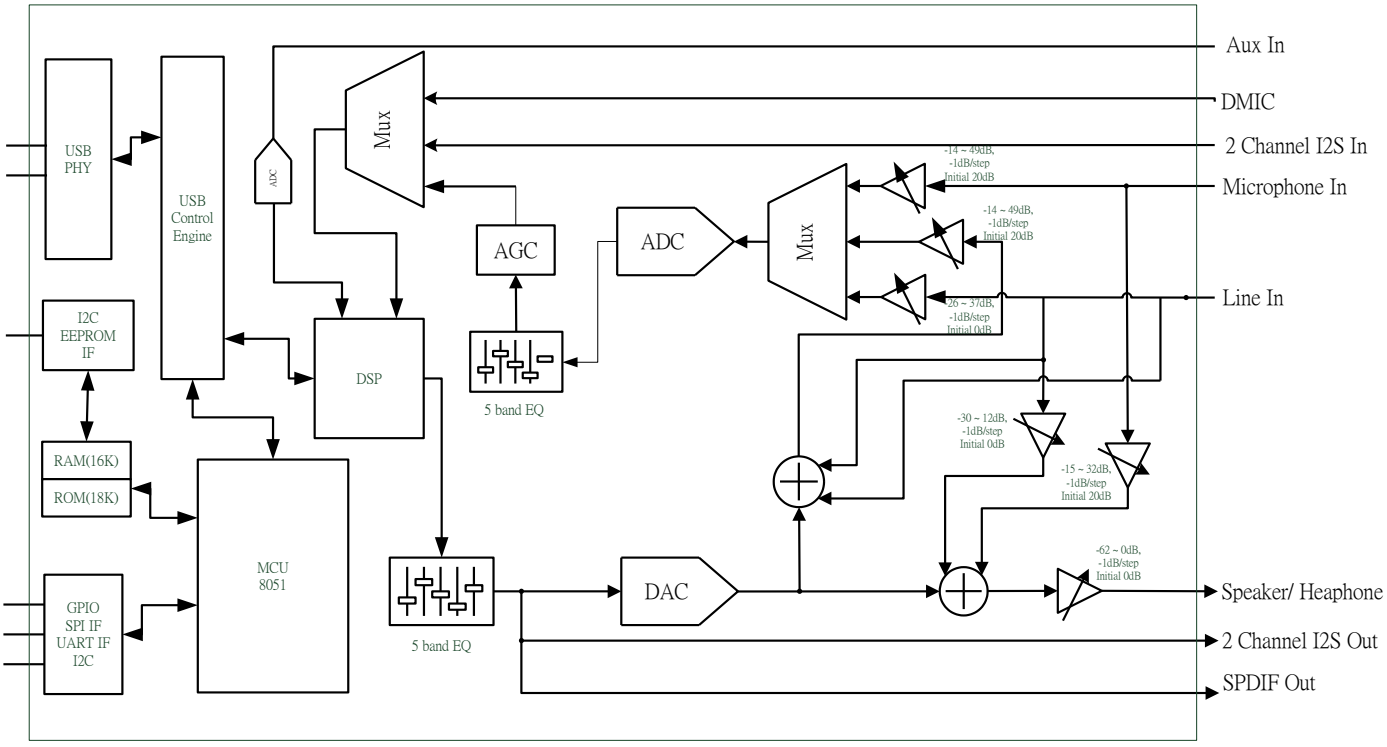
The CM6571 is a USB audio class 1.0-compatible, boasting plug and play functionality without installing additional software on popular operating systems. The internal DAC/ADC and S/PDIF out interface supports 96k/88.2k/48k/44.1kHz sampling rates and 16/24-bit resolutions.

Furthermore, the DSP inside CM6571 supports voice and audio process. Voice process includes Environment Noise Cancellation, Acoustic Echo Cancellation and Noise Reduction, functions that produce better communication experience. Audio process includes Xear™ surround headphone, sound expander, dynamic bass, audio brilliant, smart volume and parameter Equalizer, processes that enrich music playback, movie and gaming battle sound vividness.

FEATURES

- USB 2.0 full speed-compliant
- USB audio device class 1.0-compliant
- USB human interface device (HID) class 1.1-compliant
- Built-in DSP for voice and audio process
- Voice process supports ENC, AEC and NR
- Audio process supports Xear™ Surround, Sonic and parameter EQ
- Embedded 1T 8051
- Two-channel DAC for audio output interface
- Two-channel ADC for audio input interface
- Aux in for AEC signal reference
- Built-in 96k/88.2k/48k/44.1kHz and 16/24-bit S/PDIF transmitter
- Supports I2S in/out interface and up to 96kHz/24 bits
- Built-in AGC on recording path

BLOCK DIAGRAM



Release notes

Revision	Date	Description
1.0	2013/05/19	Formal release

TABLE OF CONTENTS

1 Description and overview 5
2 Ordering information 5
3 Features 5
4 Applications 8
5 Block diagram 8
6 Pin assignment 9
6.1 Pin-out diagram 9
6.2 Pin description 10
7 Application mode 13
7.1 Audio flow 13
7.1.1 recording path 13
7.1.2 playback path 13
7.2 Signal connection diagram 14
7.2.1 AEC system diagram 14
7.2.2 ENC system diagram 16
7.2.3 Array system diagram 18
7.2.4 play sound effect system diagram 20
8 USB function description 21
8.1 USB audio topology 21
8.2 Example topology –headset 21
8.3 USB HID 29
8.3.1 HID interrupt in 29
8.3.2 HID get_input_report 30
8.3.3 HID set_output_report 31
8.4 USB vender command definition 32
8.4.1 vender command read 32
8.4.2 vender command write 32
8.5 I2C interface 33
8.5.1 I2C master mode 33
8.5.1.1 I2C protocol timing 33
8.5.1.2 I2C-master read with clk_sync mode 34
8.5.2 I2C slave mode 34
8.6 I2S control description 35
8.6.1 I2S format description 35
8.6.2 I2S mclk/bclk/lrck ratio and format 37
8.7 SPDIF control description 39

8.7.1 SPDIF frame description 39
8.7.2 SPDIF out channel status 40
9 DSP function description 41
9.1 Operation modes 41
9.2 Mode state diagram and power management 42
9.3 Recommended control methods for DSP core 44
9.3.1 scenario I 44
9.3.2 scenario II 45
9.3.3 scenario III 46
9.4 Power level description table of DSP 47
10 Electrical characteristics 48
10.1 Absolute maximum ratings 48
10.2 Recommended operation conditions 48
10.3 Power consumption 48
10.4 DC characteristics 48
10.5 Audio performance 49
10.5.1 DAC audio quality 49
10.5.2 ADC audio quality 54
10.5.3 A-A path audio quality 60
10.5.4 DSP audio quality 62
11 Package dimensions 63

1 Description and overview

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2 Ordering information

Product	Package Marking	Package Type	Transport Media	Storage Temperature
CM6571	CM6571	VQFN-88 (10 x 10mm) Green Package	Tray	-45 to 120℃

3 Features

3.1 USB compliance

- USB specification 2.0 full speed-compatible
- Three USB upstream ports for connecting to a PC and mobile device simultaneously
- USB audio device class 1.0-compliant
- USB human interface device (HID) class 1.1-compliant
- Supports USB suspend/resume/reset functions
- Supports control/interrupt/bulk/isochronous data transfers

3.2 DSP algorithm

- Voice process
  - Xear™ Volear Environment Noise Cancellation (ENC) technology for dual omni-microphones
  - Adjustable 20-40dB cancellation of environmental dynamic and stationary noises and other parameters
  - Supports mic auto-calibration mechanism, allowing dual-mic sensitivity and mismatching in production
  - Allows wide placement distance range between two microphones (8-14 cm recommended)
  - Supports mic-in auto-gain control (AGC) for ADC recording quality when the ENC function is on
  - Optional acoustic echo cancellation (AEC) processing mode for speakerphones
  - Optional mono-mic noise reduction (NR) processing mode for camcorder/voice recorders
  - 16-bit/16kHz high-fidelity voice processing
- Audio process
  - Xear™ surround headphone

- Xear™ sound expander
- Xear™ Sonic
  - Dynamic bass
  - Audio brilliant
  - Smart volume
- Parameter Equalizer

3.3 Audio engine

- Playback streams:
  - Stereo DAC
    - sample rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/88.2K/96K
    - Supported bit lengths: 16 bits and 24 bits
    - Gain Range: -62dB ~ 0dB, 1dB/step
  - I2S out interface
    - sample rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/88.2K/96K
    - Supported bit lengths: 16 bits and 24 bits
    - Gain Range: -62dB ~ 0dB, 1dB/step
  - SPDIF out
    - sample rates: 44.1K/48K/88.2K/96K
    - Supported bit lengths: 16 bits and 24 bits
- Capture streams:
  - Stereo ADC
    - Default sample rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/88.2K/96K
    - Supported bit lengths: 16 bits and 24 bits
  - I2S data input
    - sample rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/88.2K/96K
    - Supported bit lengths: 16 bits and 24 bits
    - Gain Range: -62dB ~ 0dB, 1dB/step

3.4 Audio I/O

- One I2S or left-justified serial audio output interface
- One I2S or left-justified serial audio input interface
- Two-channel microphone in
- Two-channel digital microphone in
- Two-channel line in
- Two-channel line out

- S/PDIF transmitter
- Aux in

3.5 Integrated 8051 microprocessor

- Embedded 8051 microprocessor to handle comment/protocol transactions
- Connects to an external EEPROM memory for firmware codes
- HID interrupts can be implemented via firmware codes
- Provides maximum HW configuration flexibility with firmware code upgrade
- VID/PID/product strings can be customized via firmware code programming

3.6 Control interface

- Master I2C control interface for external audio devices or EEPROM access
- Maximum of 15 GPIO pins can be configured via firmware programming
- GPIOs set to HID key, LED indicator and IR receiver configurations

3.7 General

- HW EQ for both playback and record paths
- Single 12MHz crystal input is required only (embedded PLL function)
- Single 5V power supply (embedded 5V to 1.8V regulator for digital core, 5V to 3.3V regulator for digital IO, 5V to 3.5V regulator for analog codec)
- 3.3V digital I/O pads with 5V tolerance
- Industry-standard VQFN-88 package (10x10mm)

Note:
CM6571 is a USB 2.0 full speed audio device. Since bandwidth limitation, CM6571 can't support 96KHz/24btis for playback and capture streams simultaneously. The possible combinations are as below table.

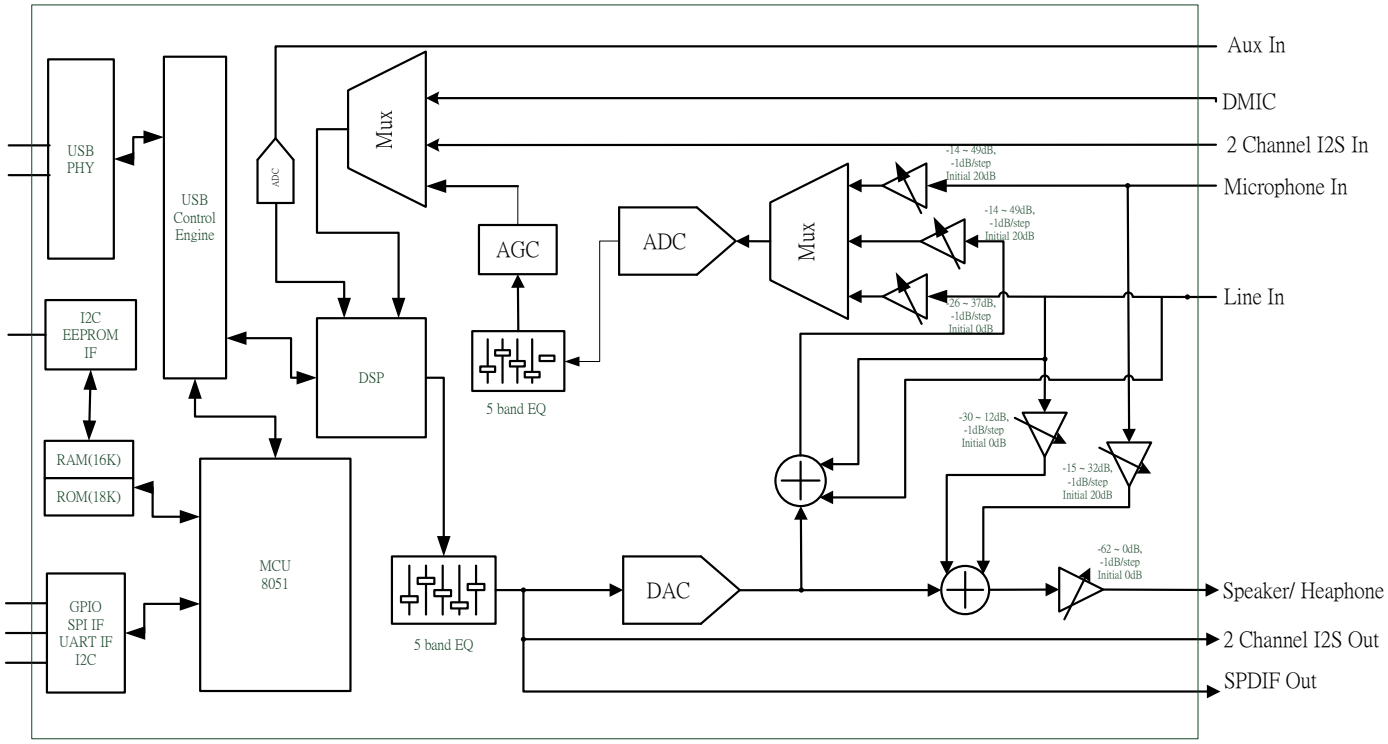
	Playback	Capture
Audio Format	96KHz/24bits	48kHz/24bits or below
	48K/24bits or below	96KHz/24bits

And for best compatibility in different OS, the default input and output audio format support up to 48KHz and 16bits. 96KHz/24bits can be enabled by firmware update.

4 Applications

- Speakerphone with acoustic echo cancellation
- USB speaker with sound expander and Xear™ sound effect
- Skype TV module with AEC + LDR
- USB headset with ENC
- USB gaming headset with Xear™ sound effect
- iDevice docking with Xear™ sound effect
- Audio boxes
- USB array/beam forming microphone

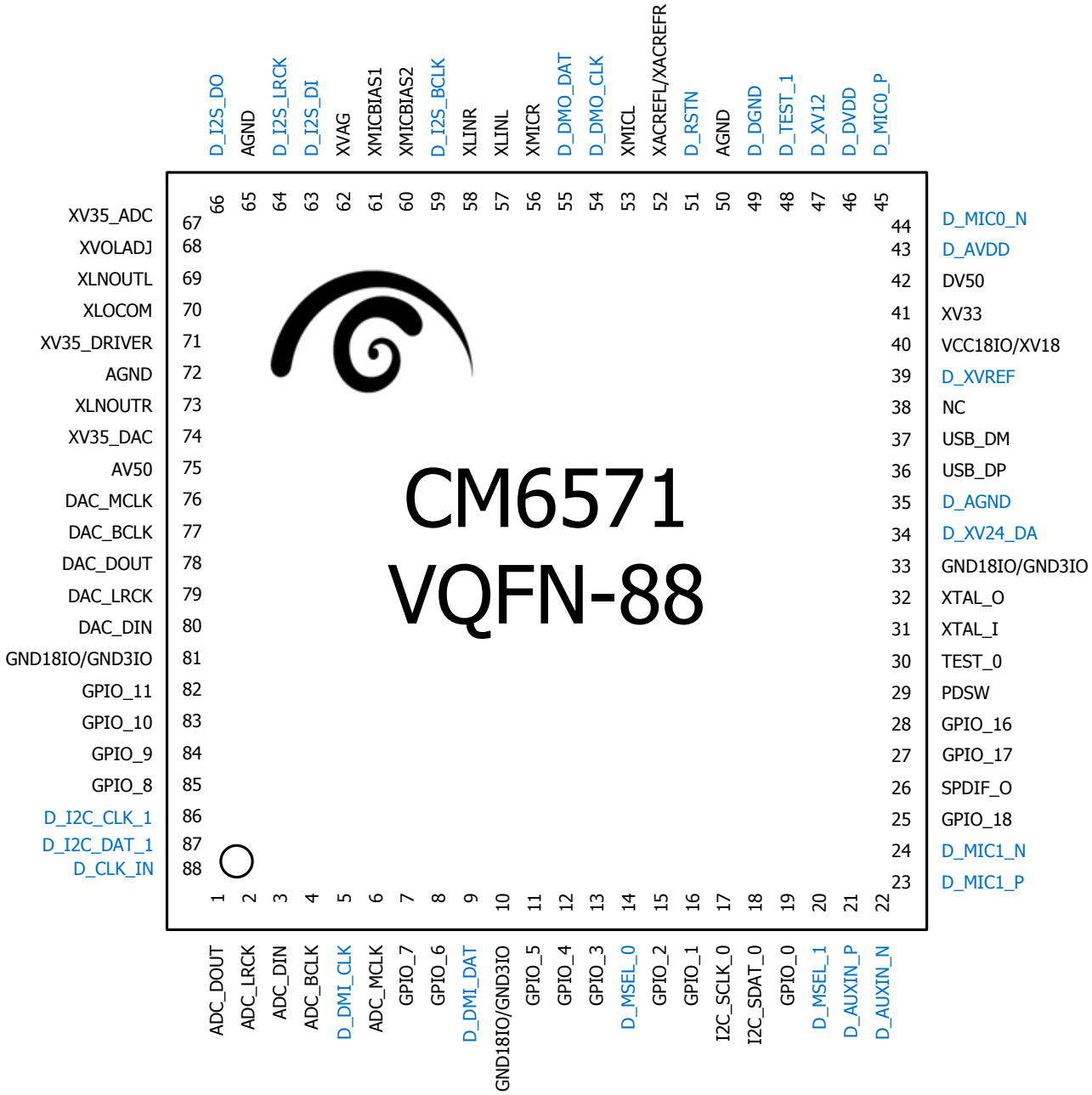
5 Block diagram



CM6571 Functional Block Diagram

6 Pin assignment

6.1 Pin-out diagram



6.2 Pin description

Pin #	Symbol	I/O	Description
Clock			
32	XTAL_O	AO	12MHz crystal oscillator output
31	XTAL_I	AI	12MHz crystal oscillator input
88	D_CLK_IN	DI, PD	Clock input (default 26MHz, configurable for 1~31MHz)
USB 2.0 BUS Interface			
37	USB_DM	AIO	USB 2.0 data negative (USB D- signal)
36	USB_DP	AIO	USB 2.0 data positive (USB D+ signal)
Power/Ground			
42	DV50	PWR	5V digital power for 5/3.3 regulator
40	VCC18IO	AO	1.8V power for digital I/O and core
41	XV33	AO	Regulator 3.3V output, drive capacity 150mA for USB and digital I/O
10	GND18IO/GND3IO	GND	Digital ground
33	GND18IO/GND3IO	GND	Digital ground
81	GND18IO/GND3IO	GND	Digital ground
75	AV50	PWR	5V analog power for 5/3.5 regulator
50	AGND	GND	Analog ground
65	AGND	GND	Analog ground
72	AGND	GND	Analog ground
74	XV35_DAC	AO	Regulator 3.5V output, drive capacity 100mA for analog and amplifier
67	XV35_ADC	AO	3.5V power for ADC and voltage and current reference
71	XV35_DRIVER	AO	3.5V power for driver
34	D_XV24_DA	AIO	Regulator capacitor filter for analog circuit
35	D_AGND	GND	Analog ground
43	D_AVDD	PWR	Analog power
39	D_XVREF	AO	Voltage reference capacitor filter
46	D_DVDD	PWR	Digital power
47	D_XV1.2	AIO	Regulator capacitor filter for digital and PLL circuit
49	D_DGND	PWR	Digital ground
Audio Interface			
52	XACREFL/XACREFR	AO	Common reference voltage for input signal
53	XMICL	AI	Mic in: left channel
56	XMICR	AI	Mic in: right channel
57	XLINL	AI	Line in: left channel
58	XLINR	AI	Line in: right channel
60	XMICBIAS2	AO	Microphone bias, 2.75V
61	XMICBIAS1	AO	Microphone bias, 2.75V
62	XVAG	AO	Voltage reference cap filter
68	XVOLADJ	AI	Analog control voltage input for playback volume control
69	XLNOUTL	AO	Line out: left channel
70	XLOCOM	AO	Line out: common reference for capless connection
73	XLNOUTR	AO	Line out: right channel
21	D_AUXIN_P	AI	Differential analog aux line input P
22	D_AUXIN_N	AI	Differential analog aux line input N
23	D_MIC1_N	AI	Differential analog microphone 1 input N
24	D_MIC1_P	AI	Differential analog microphone 1 input P
44	D_MIC0_N	AIN	Differential analog microphone 0 input N
45	D_MIC0_P	AIN	Differential analog microphone 0 input P
2-channel I2S DAC Interface			
76	DAC_MCLK	DO	I2S master clock Programmable 3.3V output buffer

77	DAC_BCLK	DIO	I2S bit clock Programmable 3.3V bidirectional buffer, pull-down
78	DAC_DOUT	DO	I2S serial data output for channels 0 and 1 Programmable 3.3V output buffer
79	DAC_LRCK	DIO	I2S left/right clock Programmable 3.3V bidirectional buffer, pull-down
80	DAC_DIN	DI	Input from DSP to DAC for playback
2-channel I2S Interface			
59	D_I2S_BCLK	DI	I2S bit clock
63	D_I2S_DI	DI	I2S serial data input
64	D_I2S_LRCK	DI	I2S left/right clock
66	D_I2S_DO	DO	I2S serial data output
Digital Microphone interface			
5	D_DMI_CLK	DO	Digital microphone clock output
9	D_DMI_DAT	DI	Digital microphone data input
54	D_DMO_CLK	DI	Digital microphone clock input
55	D_DMO_DAT	DO	Digital microphone data output
2-channel I2S ADC interface			
1	ADC_ DOUT	DO	Output from ADC to DSP for data processing
2	ADC_ LRCK	DIO	I2S left/right clock Programmable 3.3V bidirectional buffer, pull-down
3	ADC_ DIN	DI	I2S serial data input for channel 0, 1 Programmable 3.3V input buffer, Schmitt trigger, pull-down
4	ADC_ BCLK	DIO	I2S bit clock Programmable 3.3V bidirectional buffer, pull-down
6	ADC_ MCLK	DO	I2S master clock Programmable 3.3V output buffer
S/PDIF I/O			
26	SPDIF_O	DO	S/PDIF transmitter Programmable 3.3V output buffer
GPIO			
19	GPIO_0	DIO	General purpose input/output (default Volume Up) Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
16	GPIO_1	DIO	General purpose input/output (default Volume Down) Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
15	GPIO_2	DIO	General purpose input/output (default Play Mute) Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
13	GPIO_3	DIO	General purpose input/output (default Rec Mute) Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
12	GPIO_4	DIO	General purpose input/output (default LED Live, 2K Hz) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
11	GPIO_5	DIO	General purpose input/output (default LED Play Mute) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
8	GPIO_6	DIO	General purpose input/output (default LED Rec Mute, 1K Hz) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
7	GPIO_7	DIO	General purpose input/output (default EQ mode select 0) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
85	GPIO_8	DIO	General purpose input/output (default EQ mode select 1) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
			GPIO[8:7]=0,0: Normal GPIO[8:7]=1,0: Communication GPIO[8:7]=0,1: Gaming GPIO[8:7]=1,1: Movie
84	GPIO_9	DIO	General purpose input/output (default Rec Clip Indicator) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
83	GPIO_10	DIO	General purpose input/output (default Wave Volume Up) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down

82	GPIO_11	DIO	General purpose input/output (default Wave Volume Down) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
28	GPIO_16	DIO	General purpose input/output (default MCU_RXD) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down Output high voltage, 2.4V
27	GPIO_17	DIO	General purpose input/output (default MCU_TRX) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down Output high voltage, 2.4V
25	GPIO_18	DIO	General purpose input/output (default IR Module) Programmable 3.3V/5V tolerance bidirectional buffer, pull-down Output high voltage, 2.4V
2-Wire Master Serial Bus (I2C)			
18	I2C_SDAT_0	DIO	2-wire master serial data Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
17	I2C_SCLK_0	DIO	2-wire master serial clock Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
86	D_I2C_CLK_1	DIO, PU	I2C clock
87	D_I2C_DAT_1	DIO, PU	I2C data
Miscellaneous			
29	PDSW	DO	Power Down switch Normal: 0 Suspend: 1
30	TEST_0	DI	For testing
48	D_TEST_1	DI	For testing
38	NC		
14	D_MSEL_0	DI	Mode selector values (MSEL_1, MSEL_0): 0x00: Power Down (default) 0x01: active (ENC ON/AEC/NR) 0x11: by-pass mode (effect off) 0x10: suspend
20	D_MSEL_1	DI	
51	D_RSTN	DI, PU	Chip reset input, low active

Note: Pin name with “D” character means DSP pin out.

7 Application mode

7.1 Audio flow

7.1.1 Recording path

Functions		Input path(Recording)							
Input	AEC	(USB side) Mic in	Dmic clk (GPIO10), Dmic data(GPIO11) Analog mic(XMICL, XMICR)	L: Mic input R: reference signal	(USB side) I2S-in Dout (ADC_DOUT)	(DSP side) I2S Din(I2S_DI)	(DSP side) I2S Dout(I2S_DO)	(USB side) I2S-in Din (ADC_DIN)	USB
		(DSP side) Mic in	Dmic clk (DMI_CLK), Dmic data(DMI_DAT) Analog mic (MIC0_N/P, MIC1_N/P)	MIC0: Mic input, MIC1: reference signal	(DSP side)Dmic out(DMO_CLK, DMO_DAT)	(USB side)Dmic in(GPIO10, GPIO11)		USB	
	ENC	(USB side) Mic in	Dmic clk (GPIO10), Dmic data(GPIO11) Analog mic(XMICL, XMICR)	L, R are for two mic input	(USB side) I2S-in Dout (ADC_DOUT)	(DSP side) I2S Din(I2S_DI)	(DSP side) I2S Dout(I2S_DO)	(USB side) I2S-in Din (ADC_DIN)	USB
		(DSP side) Mic in	Dmic clk (DMI_CLK), Dmic data(DMI_DAT) Analog mic(MIC0_N/P, MIC1_N/P)	Mic 0, 1	(DSP side)Dmic out(DMO_CLK, DMO_DAT)	(USB side)Dmic in(GPIO10, GPIO11)		USB	
	Array	(USB side)Mic in	Dmic clk(GPIO10), Dmic data(GPIO11) Analog mic(XMICL, XMICR)	L, R are for two mic input	(USB side) I2S-in Dout (ADC_DOUT)	(DSP side) I2S Din(I2S_DI)	(DSP side) I2S Dout(I2S_DO)	(USB side) I2S-in Din (ADC_DIN)	USB
		(DSP side) Mic in	Dmic clk (DMI_CLK), Dmic data(DMI_DAT) Analog mic(MIC0_N/P, MIC1_N/P)	Mic 0,1	(DSP side)Dmic out(DMO_CLK, DMO_DAT)	(USB side)Dmic in(GPIO10, GPIO11)		USB	

7.1.2 playback path

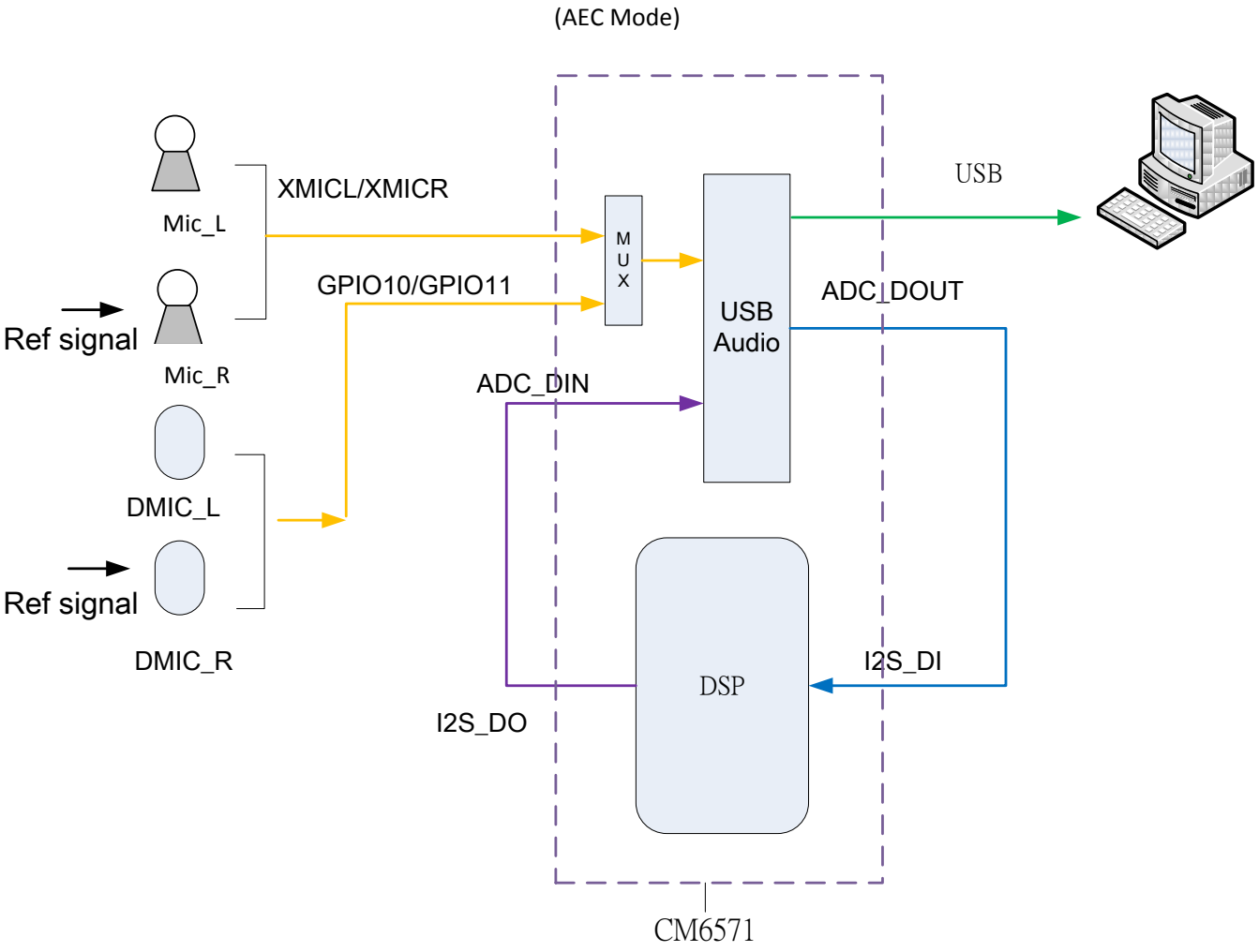
Functions		output path(playback)					
Output	surround HP	USB	(USB side) I2S-out Dout(DAC_DOUT)	(DSP side)I2S Din (I2S_DI)	(DSP side)I2S Dout (I2S_DO)	(USB side) I2S-out Din(DAC_DIN)	(USB side) analog out(XLNOUTL/XLNOUTR)
	sound expander	USB	(USB side) I2S-out Dout(DAC_DOUT)	(DSP side)I2S Din (I2S_DI)	(DSP side)I2S Dout (I2S_DO)	(USB side) I2S-out Din(DAC_DIN)	(USB side) analog out(XLNOUTL/XLNOUTR)
	Xear sonic	USB	(USB side) I2S-out Dout(DAC_DOUT)	(DSP side)I2S Din (I2S_DI)	(DSP side)I2S Dout (I2S_DO)	(USB side) I2S-out Din(DAC_DIN)	(USB side) analog out(XLNOUTL/XLNOUTR)
	parameter EQ	USB	(USB side) I2S-out Dout(DAC_DOUT)	(DSP side)I2S Din (I2S_DI)	(DSP side)I2S Dout (I2S_DO)	(USB side) I2S-out Din(DAC_DIN)	(USB side) analog out(XLNOUTL/XLNOUTR)

7.2 Signal connection diagram

7.2.1 AEC system diagram

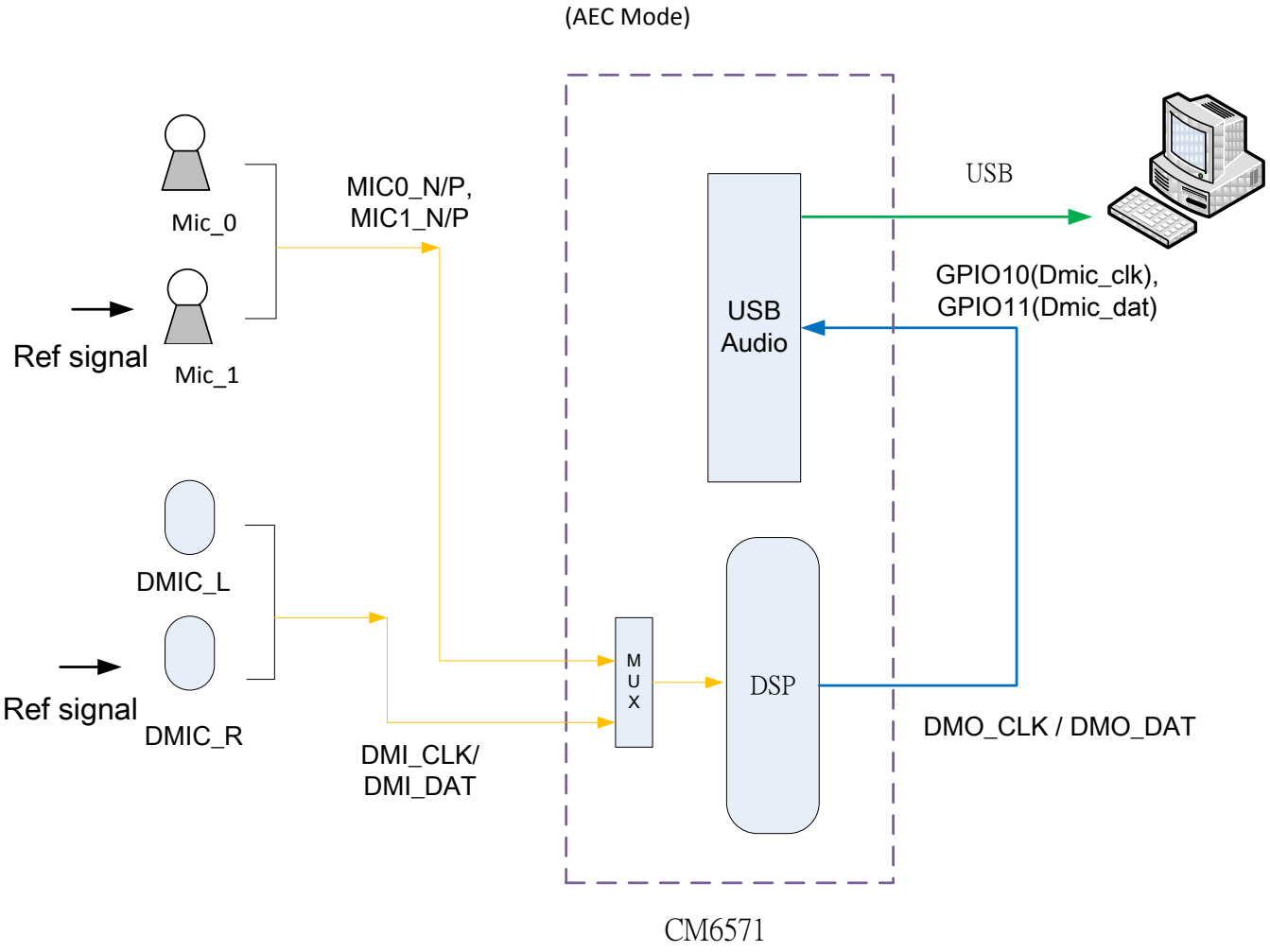
7.2.1.1 from USB side input

Path: USB Audio Microphone in→ USB Audio I2S In(D out)→DSP I2S in→DSP I2S out→USB Audio I2S In(D in)→ USB → PC



7.2.1.2 from DSP side input

Path: DSP Microphone in→ DSP digital microphone out→ USB Audio digital microphone in→ USB → PC



DMIC_R

I2S_DO

DSP

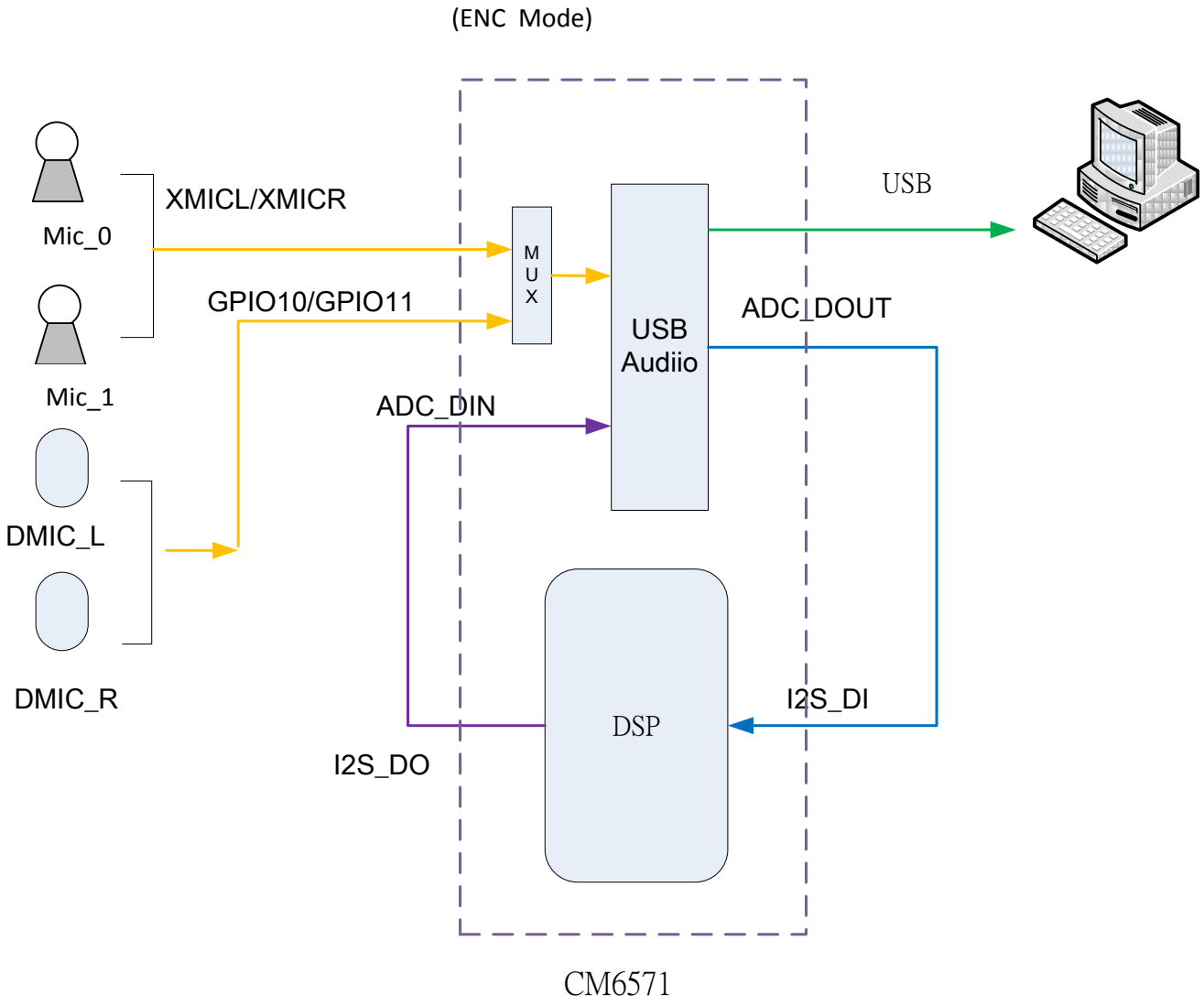
I2S_DI

CM6571

7.2.2 ENC system diagram

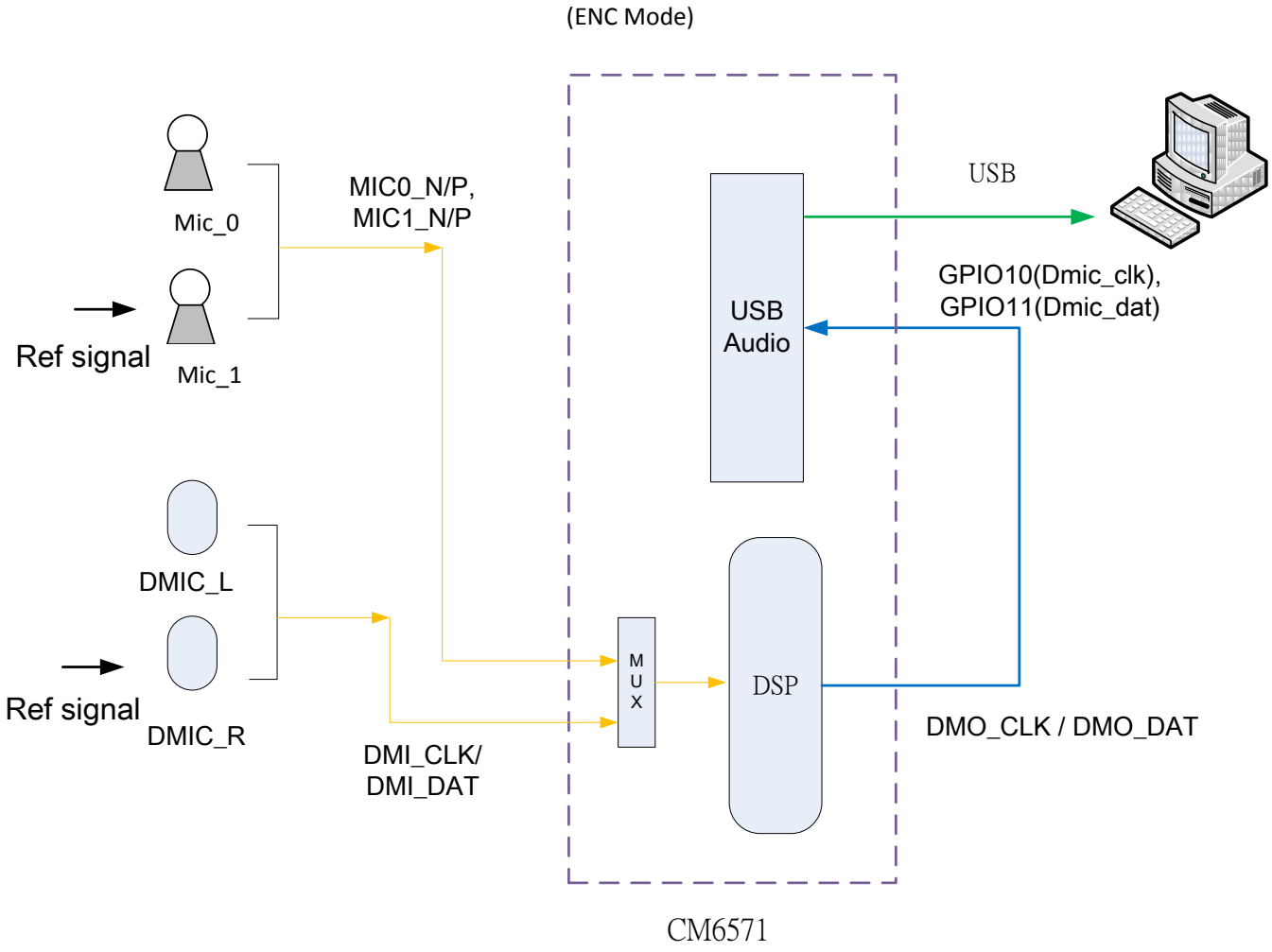
7.2.2.1 from USB side input

Path: USB Audio Microphone in→ USB Audio I2S In(D out)→DSP I2S in→DSP I2S out→USB Audio I2S In(D in)→ USB → PC



7.2.2.2 from DSP side input

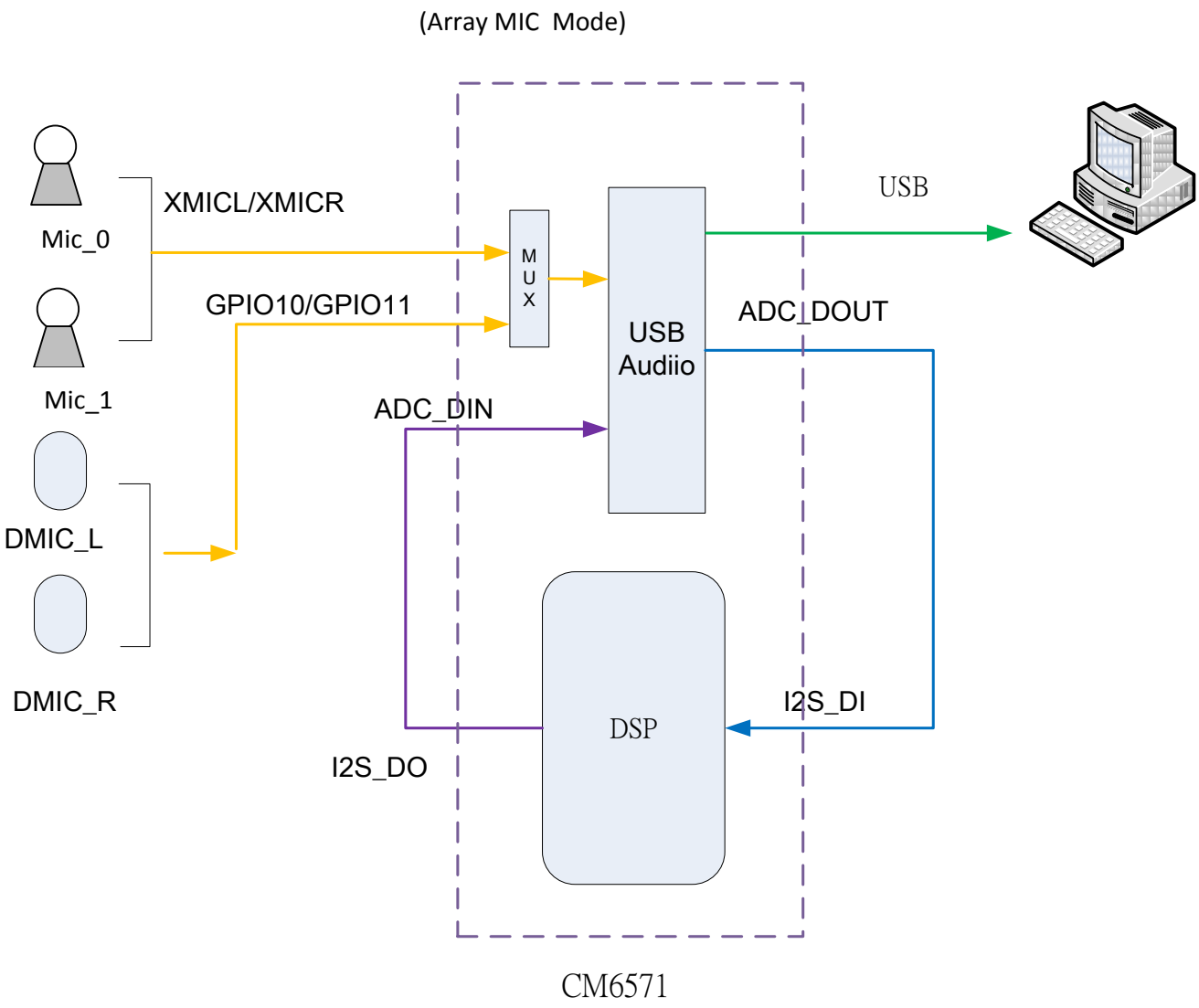
Path: DSP Microphone in→ DSP digital microphone out→ USB Audio digital microphone in→ USB → PC



7.2.3 Array system diagram

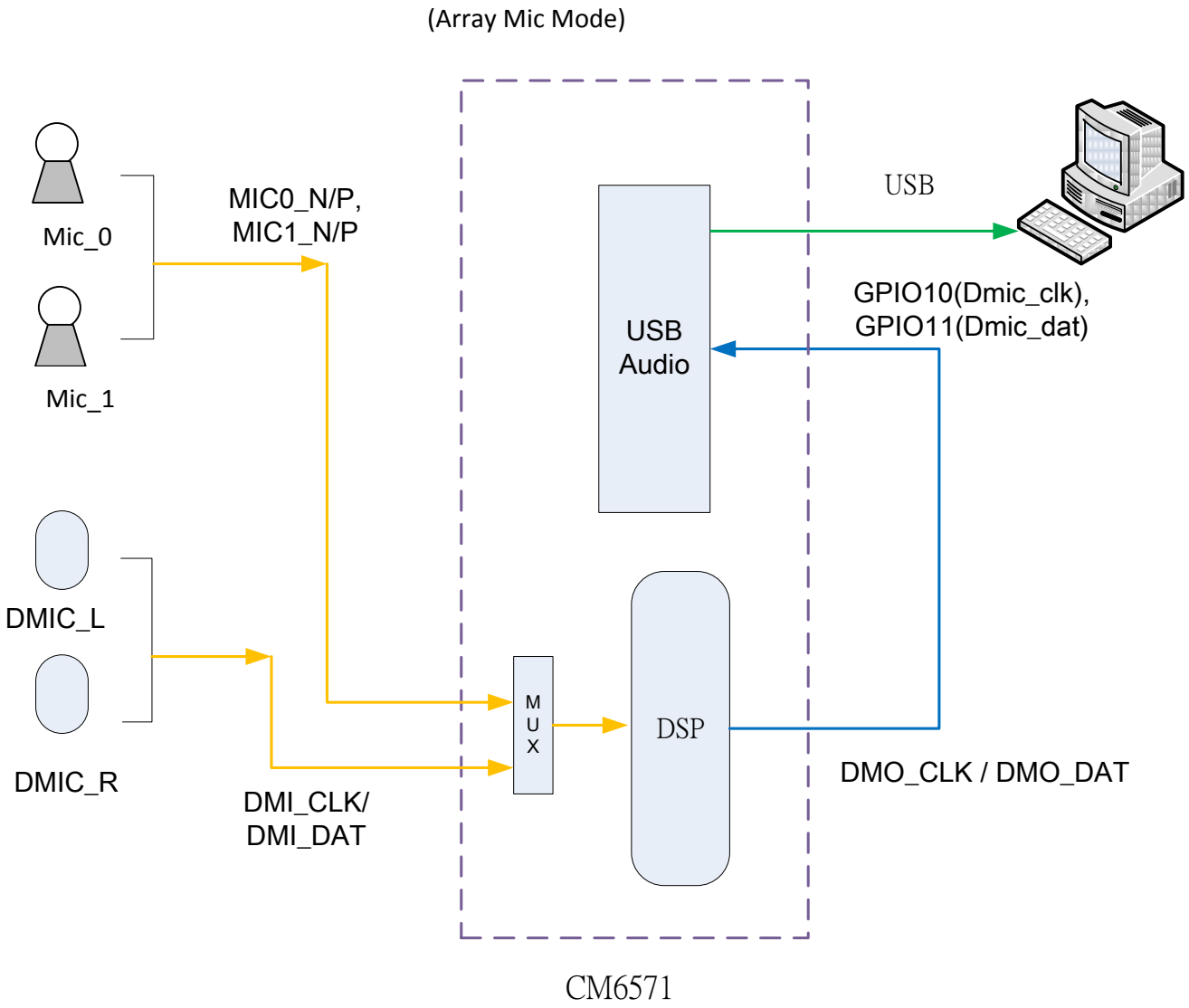
7.2.3.1 from USB side input

Path: USB Audio microphone in→ USB I2S in(D out)→DSP I2S in→DSP I2S out →USB Audio I2S In(D In)→ USB → PC



7.2.3.2 from DSP side input

Path: DSP microphone in→ DSP digital microphone out→ USB Audio digital microphone in→ USB → PC

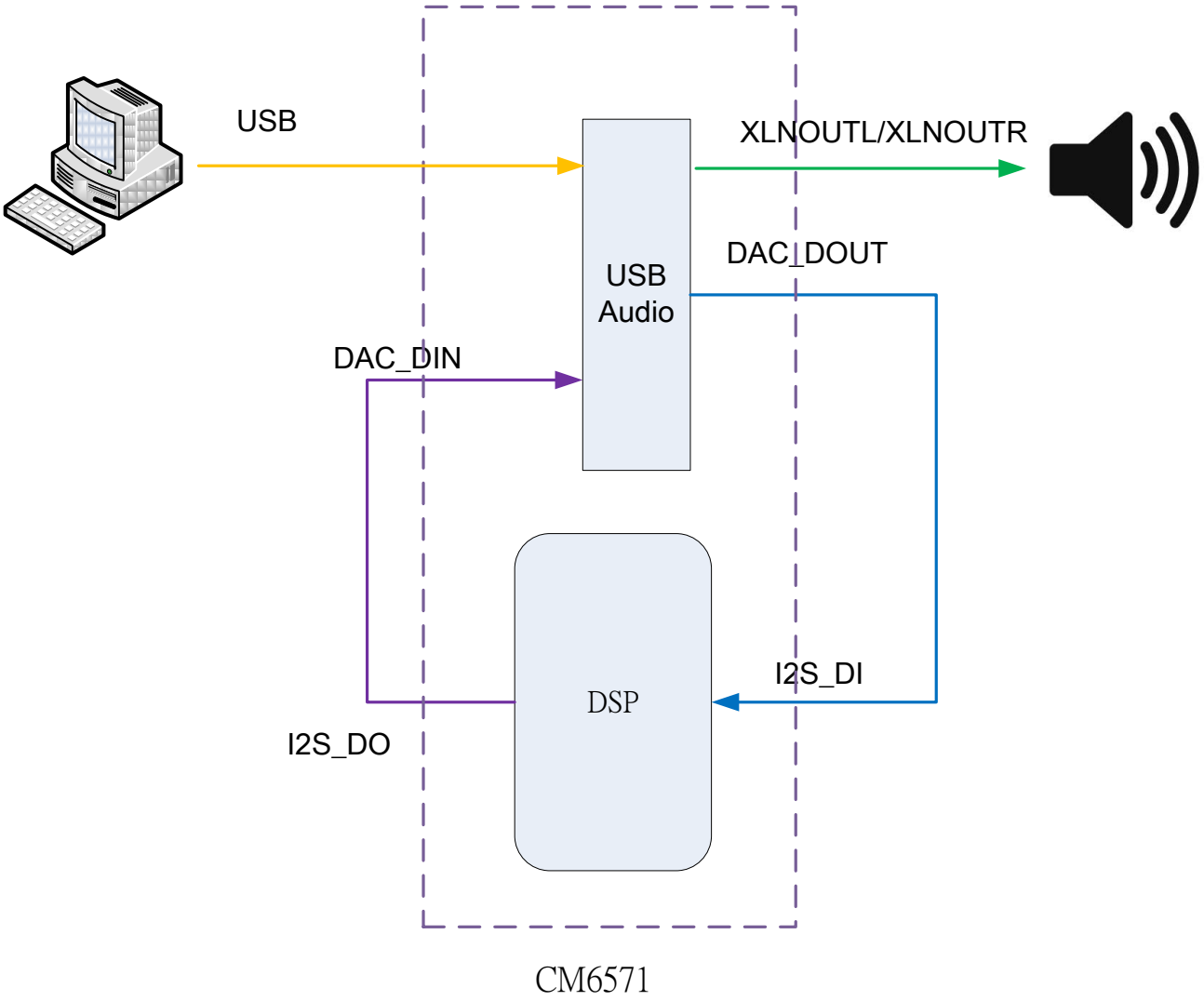


7.2.4 play sound effect system diagram

(surround HP/sound expander/Xear™ sonic/parameter EQ)

Path: PC→USB→USB Audio→ USB Audio I2S out(D out)→ DSP I2S in→ DSP I2S out→ USB Audio I2S out(D in)→ USB Audio Line out →Speaker

(play sound effect Mode)

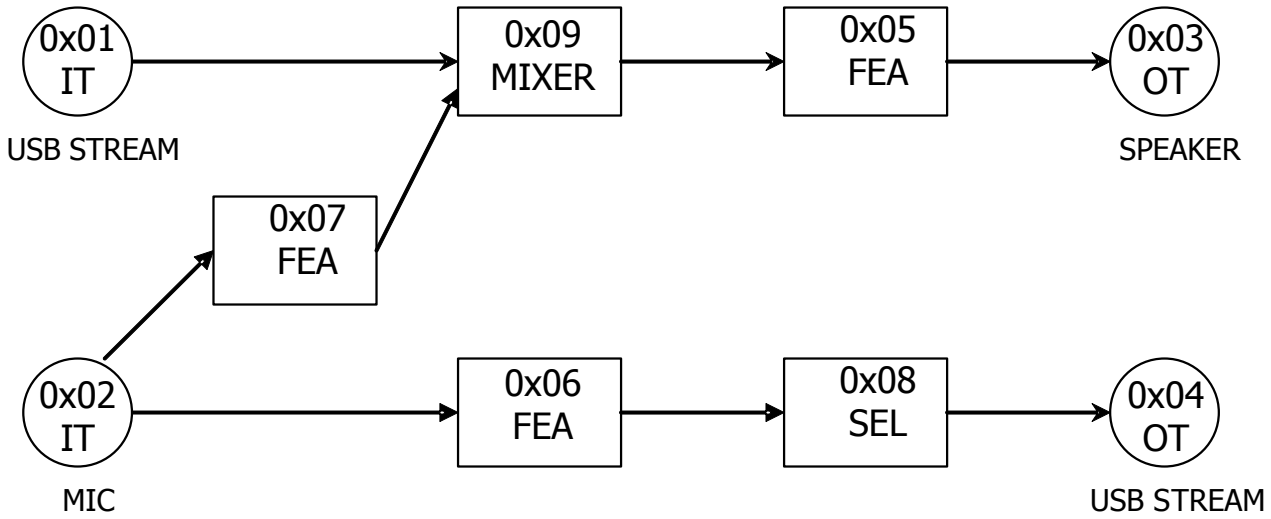


8 USB function description

8.1 USB audio topology

The MCU of CM6571 can use internal ROM code or download customized code to implement USB audio device in different topologies. This USB device can provide one control pipe, two ISO IN/OUT pipes, one interrupt pipe and four BULK IN/OUT pipes.

8.2 Example topology –headset



device descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	10	Endpoint zero packet size
8	idVendor	2	0D8C	Vendor ID
10	idProduct	2	0178~017F	Product ID
12	bcdDevice	2	0000	Device release number
14	iManufacturer	1	01	Index of string descriptor describing manufacturer
15	iProduct	1	02	Index of string descriptor describing product
16	iSerialNumber	1	00	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

configuration descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	011D	Total length of data returned for this configuration: 285 Bytes
4	bNumInterfaces	1	04	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: ISO-In 03: INT-In (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	80	Attributes(Bus Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1)

audio control interface 0 descriptor 0

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	00	Interface number
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	01	Subclass code: AUDIO_CONTROL
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

class-specific AC interface header descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0A	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	01	HEADER descriptor subtype
3	bcdADC	2	0100	Audio Device Class specification release number
5	wTotalLength	2	0066	Total length of data returned for the class-specific Audio Control interface descriptor:
7	bInCollection	1	02	The number of Audio Stream interfaces in the collection: 02
8	baInterfaceNr(1)	1	01	Interface number of the first Audio Stream interface in the collection
9	baInterfaceNr(2)	1	02	Interface number of the second Audio Stream interface in the collection

class-specific input terminal descriptor (USB stream), ID=01

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0C	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	02	INPUT_TERMINAL descriptor subtype
3	bTerminalID	1	01	Terminal ID
4	wTerminalType	2	0101	Terminal Type: USB Stream
6	bAssocTerminal	1	00	Associate Terminal
7	bNrChannels	1	02	Number of channel Stereo : 02
8	wChannelConfig	2	0003	D0: Left Front (L) D1: Right Front (R)
10	iChannelNames	1	00	Index of string descriptor describing the name of the first logical channel

11	iTerminal	1	00	Index of string descriptor describing this Input Terminal

class-specific input terminal descriptor (microphone), ID=02

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0C	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	02	OUTPUT_TERMINAL descriptor subtype
3	bTerminalID	1	02	Terminal ID
4	wTerminalType	2	0201	Terminal Type: Microphone
6	bAssocTerminal	1	00	Associate Terminal
7	bNrChannels	1	02	Number of channel Stereo : 02
8	wChannelConfig	2	0003	D0: Left Front (L) D1: Right Front (R)
10	iChannelNames	1	00	Index of string descriptor describing the name of the first logical channel
11	iTerminal	1	00	Index of string descriptor describing this Input Terminal

class-specific output terminal descriptor (speaker),ID=03

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	03	OUTPUT_TERMINAL descriptor subtype
3	bTerminalID	1	03	Terminal ID
4	wTerminalType	1	0301	Terminal Type: Speaker
5	bAssocTerminal	1	00	Associate Terminal
6	bSourceID	1	05	Source ID: 05
8	iTerminal	1	00	Index of string descriptor describing this Output Terminal

class-specific output terminal descriptor (USB stream), ID=04

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	03	OUTPUT_TERMINAL descriptor subtype
3	bTerminalID	1	04	Terminal ID
4	wTerminalType	2	0101	Terminal Type: USB Stream
6	bAssocTerminal	1	00	Associate Terminal
7	bSourceID	1	08	Source ID: 08
8	iTerminal	1	00	Index of string descriptor describing this Output Terminal

class-specific feature unit descriptor (speaker playing) , ID=05

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0A	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	06	FEATURE_UNIT descriptor subtype
3	bUnitID	1	05	Unit ID
4	bSourceID	1	09	Source ID from Input Unit: 09
5	bControlSize	1	01	Size in byte of bmaControls array: 1 bytes
6	bmaControls(1)	1	01	master mute 01
7	bmaControls(2)	1	02	Left Front volume control 02 : stereo
8	bmaControls(3)	1	02	Right Front volume control 02 : stereo
9	iFeature	1	00	Index of string descriptor describing this Feature Unit

class-specific feature unit descriptor (microphone recording) , ID=06

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0A	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	06	FEATURE_UNIT descriptor subtype
3	bUnitID	1	06	Unit ID
4	bSourceID	1	02	Source ID from Input Unit: 02
5	bControlSize	1	01	Size in byte of bmaControls array: 1 bytes
6	bmaControls(1)	1	01	master mute 01
7	bmaControls(2)	1	02	Left Front volume control 02 : stereo
8	bmaControls(3)	1	02	Right Front volume control 02 : stereo
9	iFeature	1	00	Index of string descriptor describing this Feature Unit

class-specific feature unit descriptor (microphone recording) , ID=07

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0A	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	06	FEATURE_UNIT descriptor subtype
3	bUnitID	1	07	Unit ID
4	bSourceID	1	02	Source ID from Input Unit: 02
5	bControlSize	1	01	Size in byte of bmaControls array: 1 bytes
6	bmaControls(1)	1	01	master mute 01
7	bmaControls(2)	1	02	Left Front volume control 02 : stereo
8	bmaControls(3)	1	02	Right Front volume control 02 : stereo
9	iFeature	1	00	Index of string descriptor describing this Feature Unit

class-specific selector unit descriptor (USB stream), ID=08

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	05	SELECTOR_UNIT descriptor subtype
3	bUnitID	1	08	Unit ID
4	bNrInPins	1	01	Number of input pin
5	bmaControls(1)	1	06	Microphone Feature
6	iSelector	1	00	Index of string descriptor describing this Selector Unit

class-specific mixer unit descriptor (speaker), ID=09

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	0D	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	04	MIXER_UNIT descriptor subtype
3	bUnitID	1	09	Unit ID
4	bNrInPins	1	02	Number of input pin
5	baSourceID(1)	1	01	USB Stream
6	baSourceID(2)	1	07	Microphone Feature
7	bNrChannels	1	02	Number of output channel
8	wChannelConfig	2	0003	D0: Left Front (L) D1: Right Front (R)
10	iChannelNames	1	00	Index of string descriptor describing the name of the first logical channel
11	bmControls	1	00	All mixing controls are not programmable (this field occupies (2+2+2)*2/8 bytes)

12	iMixer	1	00	Index of string descriptor describing this Mixer Unit

standard as interface descriptor (interface 1, alternate 0)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	01	Interface number
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	02	Subclass code: AUDIO_STREAM
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

standard as interface descriptor (interface 1, alternate 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	01	Interface number
3	bAlternateSetting	1	01	Alternate interface
4	bNumEndpoints	1	01	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	02	Subclass code: AUDIO_STREAM
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

class-specific as general interface descriptor (interface 1, alternate 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	01	AS_GENERAL descriptor subtype
3	bTerminalLink	1	01	Link to Output USB Stream
4	bDelay	1	01	Sync delay: 1ms
5	wFormatTag	2	0001	PCM 16-bits format

class-specific as type format descriptor (interface 1, alternate 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	1D	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	02	Format descriptor subtype
3	bFormatType	1	01	Format type 1
4	bNrChannels	1	02	Number of channel 02 : stereo
5	bSubframeSize	1	02	2 bytes per slot
6	bBitResolution	1	10	Bit resolution : 16-bits
7	bSamFreqType	1	07	7 sampling rates
8	tSampFreq(1)	3	001F40	Sampling rate: 8kHz
11	tSampFreq(2)	3	002B11	Sampling rate: 11.025kHz
14	tSampFreq(3)	3	003E80	Sampling rate: 16kHz
17	tSampFreq(4)	3	005622	Sampling rate: 22.05kHz
20	tSampFreq(5)	3	007D00	Sampling rate: 32kHz
23	tSampFreq(6)	3	00AC44	Sampling rate: 44.1kHz
26	tSampFreq(7)	3	00BB80	Sampling rate: 48kHz

standard as ISO out audio data endpoint descriptor (ep 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	05	Endpoint Descriptor
2	bEndpointAddress	1	1	IN Endpoint, Endpoint number 1
3	bmAttributes	1	0D	ISO Endpoint, synchronous
4	wMaxPacketSize	2	0188	Maximum packet size: 392 bytes
6	bInterval	1	01	1ms
7	bRefresh	1	00	Reset to 0
8	bSynchAddress	1	00	No synchronization pipe

class-specific as ISO out audio data endpoint descriptor (ep 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	25	CS_ENDPOINT descriptor type
2	bDescriptorSubtype	1	01	EP_GENERAL descriptor subtype
3	bmAttributes	1	01	Sampling Frequency control
4	bLockDelayUnits	1	00	Reset to 0
5	wLockDelay	2	0000	No synchronization pipe

standard as interface descriptor (interface 2, alternate 0)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	02	Interface number: 02
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	02	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

standard as interface descriptor (interface 2, alternate 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	02	Interface number: 02
3	bAlternateSetting	1	01	Alternate interface
4	bNumEndpoints	1	01	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	02	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

class-specific as general interface descriptor (interface 2, alternate 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	01	AS_GENERAL descriptor subtype
3	bTerminalLink	1	04	Link to Output USB Stream
4	bDelay	1	01	Sync delay: 1ms
5	wFormatTag	2	0001	PCM 16-bits format

class-specific as type format descriptor (interface 2, alternate 1)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	1D	Descriptor length
1	bDescriptorType	1	24	CS_INTERFACE descriptor type
2	bDescriptorSubtype	1	02	Format descriptor subtype
3	bFormatType	1	01	Format type 1
4	bNrChannels	1	02	Number of channelAlways 2ch
5	bSubframeSize	1	02	2 bytes per slot
6	bBitResolution	1	10	Bit resolution: 16-bits
7	bSamFreqType	1	07	7 sampling rates
8	tSampFreq(1)	3	001F40	Sampling rate: 8kHz
11	tSampFreq(2)	3	002B11	Sampling rate: 11.025kHz
14	tSampFreq(3)	3	003E80	Sampling rate: 16kHz
17	tSampFreq(4)	3	005622	Sampling rate: 22.05kHz
20	tSampFreq(5)	3	007D00	Sampling rate: 32kHz
23	tSampFreq(6)	3	00AC44	Sampling rate: 44.1kHz
26	tSampFreq(7)	3	00BB80	Sampling rate: 48kHz

standard as ISO in audio data endpoint descriptor (ep 82)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	05	Endpoint Descriptor
2	bEndpointAddress	1	82	IN Endpoint, Endpoint number 2
3	bmAttributes	1	0D	ISO Endpoint, synchronous
4	wMaxPacketSize	2	0188	Maximum packet size: 392 bytes
6	bInterval	1	01	1ms
7	bRefresh	1	00	Reset to 0
8	bSynchAddress	1	00	No synchronization pipe

class-specific as ISO in audio data endpoint descriptor (ep 82)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	25	CS_ENDPOINT descriptor type
2	bDescriptorSubtype	1	01	EP_GENERAL descriptor subtype
3	bmAttributes	1	01	Sampling Frequency control
4	bLockDelayUnits	1	00	Reset to 0
5	wLockDelay	2	0000	No synchronization pipe

standard hid interface descriptor (interface 3, alternate 0)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	03	Interface number: 03
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	01	Number of endpoint used by this interface
5	bInterfaceClass	1	03	Audio Interface Class
6	bInterfaceSubClass	1	00	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

class-specific HID interface descriptor (interface 3, alternate 0)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version
4	bCountryCode	1	00	No country code
5	bNumDescriptors	1	01	One HID class descriptor
6	bDescriptorType	1	22	Report Descriptor
7	wDescriptorLength	2	002C	HID class descriptor length in byte: 44 bytes

standard HID interrupt in endpoint descriptor (ep 87)

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	05	Endpoint Descriptor
2	bEndpointAddress	1	87	IN Endpoint, Endpoint number: 07
3	bmAttributes	1	03	Interrupt Endpoint
4	wMaxPacketSize	2	0010	Maximum packet size: 16 bytes
6	bInterval	1	01	1ms

8.3 USB HID

8.3.1 HID interrupt in

8.3.1.1 input data format:

byte0	always 1 for org HID event report ID
byte1	for defined HID event, and each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT(slavemode int)
	bit3: SPIM_INT(mastermode int)
	bit2:I2CS_INT(slavemode int)
	bit1:I2CM_INT(mastermode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

8.3.2 HID get_input_report

8.3.2.1 command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h A1	8'h 01 (Get_Report)	16'h 01 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

*Note: The Start_Addr value in the input reported is put in the Internal Register Address 0xff. Software must set the value of Start_Addr Register to make sure Get Input Report can read the proper data you want.

8.3.2.2 input data format:

byte0	always 1 for org HID event report ID
byte1	for defined HID event, and each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT(slavemode int)
	bit3: SPIM_INT(mastermode int)
	bit2:I2CS_INT(slavemode int)
	bit1:I2CM_INT(mastermode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

8.3.3 HID set_output_report

8.3.3.1 command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 21	8'h 09 (Set_Report)	16'h 02 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

Note: Byte5 is the beginning address of the write sequence.

8.3.3.2 output data format:

byte0	always 1 for org HID event report ID
byte1	start address of write reg (H-start_addr)
byte2	start address of write reg (L-start_addr)
byte3	effective write/read data length (<=12)
byte4	write data to [start_addr]
byte5	write data to [start_addr+1]
byte6	write data to [start_addr+2]
byte7	write data to [start_addr+3]
byte8	write data to [start_addr+4]
byte9	write data to [start_addr+5]
byte10	write data to [start_addr+6]
byte11	write data to [start_addr+7]
byte12	write data to [start_addr+8]
byte13	write data to [start_addr+9]
byte14	write data to [start_addr+10]
byte15	write data to [start_addr+11]

8.4 USB vender command definition

8.4.1 vender command read

8.4.1.1 command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h C3	8'h 02 (Command 2)	16'h -- -- (Start Address of input Data)	16'h 00 00	16'h 00 - (<=64 bytes)	Data

8.4.1.2 input data format:

Byte0	Data of Reg[wValue]
Byte1	Data of Reg[wValue + 1]
Byte2	Data of Reg[wValue + 2]
…	…
Byte63	Data of Reg[wValue + 63]

8.4.2 vender command write

8.4.2.1 command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 43	8'h 01 (Command 1)	16'h -- -- (Start Address of Output Data)	16'h 00 00	16'h 00 - (<=64 bytes)	Data

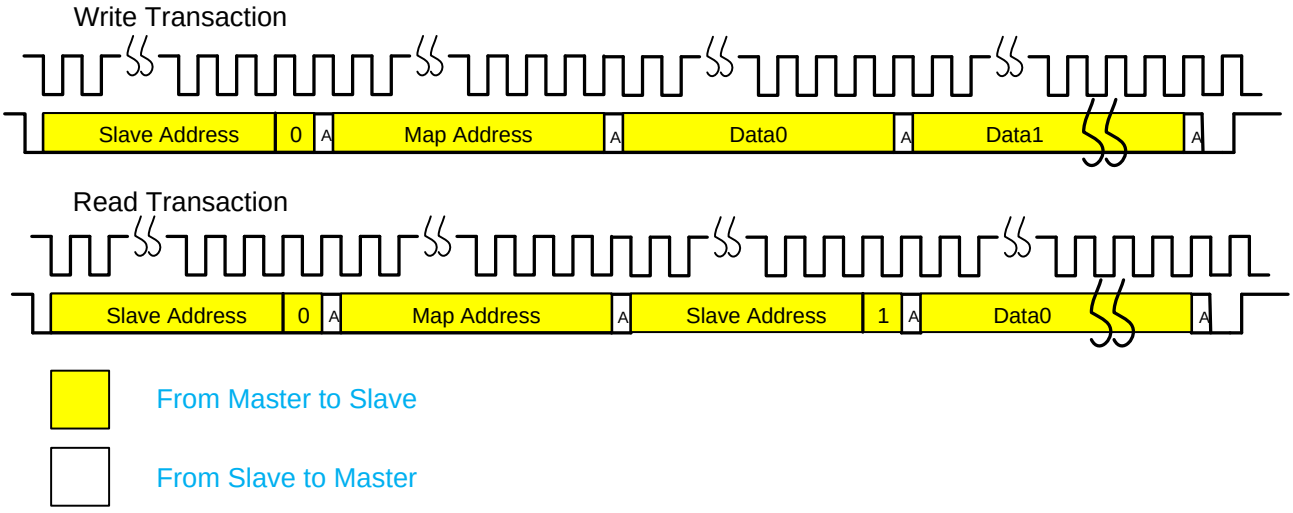
8.4.2.2 output data format:

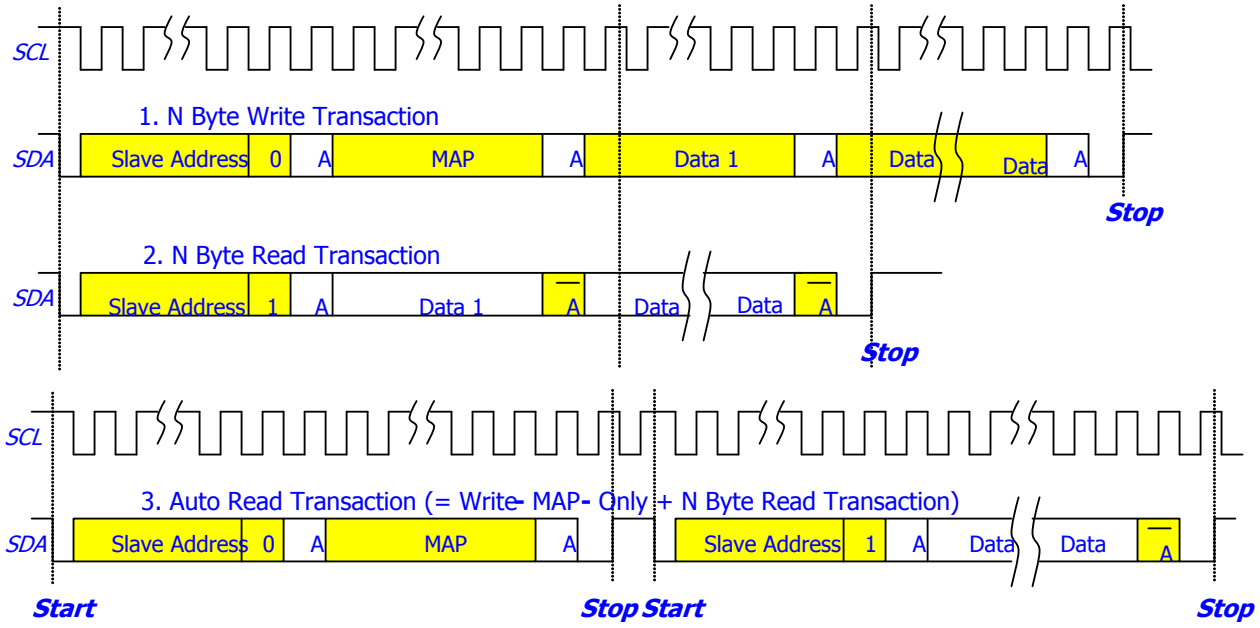
Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]

8.5 I2C interface

8.5.1 I2C master mode

8.5.1.1 I2C protocol timing





from master to slave

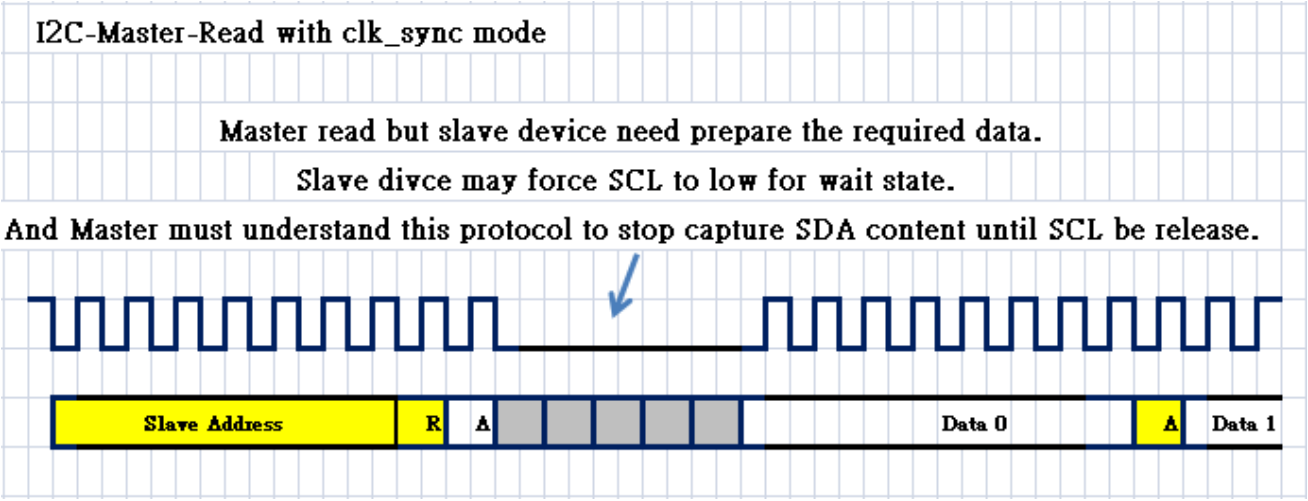
from slave to master

$A = acknowledge\ (SDA\ Low)$

$\overline{A} = not\ \ acknowledge\ (SDA\ High)$

MAP: Memory Address Pointer
(the target register address
in slave device)

8.5.1.2 I2C-master read with clk_sync mode



8.5.2 I2C slave mode

8.5.2.1 slave mode architecture

"7-bit slave address = 7'b0001000 to 7'b0001011"

The CM6571 can serve as a slave device with a bit rate of up to 400Kbps (in fast mode). An external MCU can write data to or read from the CM6571 with no size limitation in the I2C Interface. Furthermore, both the host side and the MCU have access to all the internal registers.

The CM6571 will transfer an interrupt to the internal MCU until the INT bit of the I2C control register has been cleared by the internal MCU. The interrupt is triggered when a write transaction is done, or when a slave address read is detected.

The main function of the two-wire slave bus is to be in the interface between the CM6571 and an external micro control unit (EMCU).

8.6 I2S control description

8.6.1 I2S format description

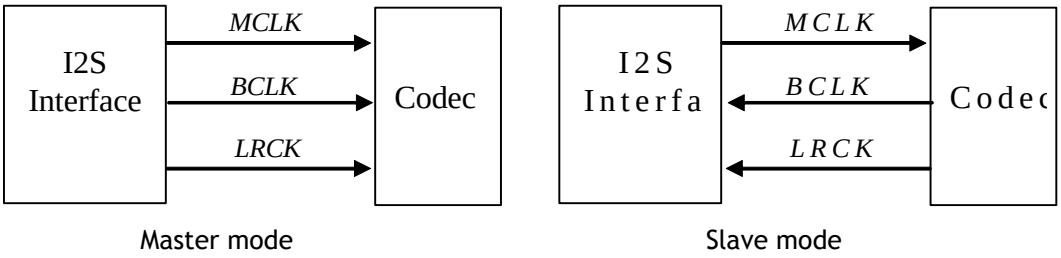
8.6.1.1 I2S interface settings

I^2S has three clock signals, MCLK, BCLK and LRCK, and one data line DOUT. The I^2S clock symbols are as follows:

- MCLK = main clock
- BCLK = bit clock
- LRCK = left and right clock

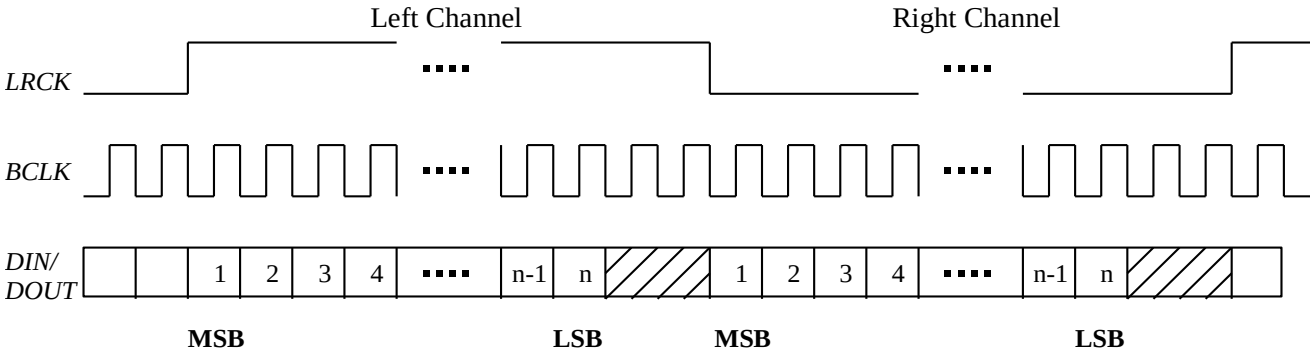
8.6.1.2 I2S bus basics

Both master and slave modes of I^2S are supported. I^2S DAC Master mode means BCLK and LRCK are provided as shown below (left). On the contrary, slave mode means BCLK and LRCK are provided by the I^2S codecs as shown below (right).



I2S MASTER/SLAVE BLOCK DIAGRAM

Below figure indicates the basic waveform of I^2S. Note that BCLK is generated at the positive edges of MCLK with the ratios 1:4, and LRCK is generated at the negative edges of BCLK with the ratios 1:64. Data lines are transited at the negative edges of BCLK and are sampled at the positive edges of BCLK by codecs in the case of playback or recording.

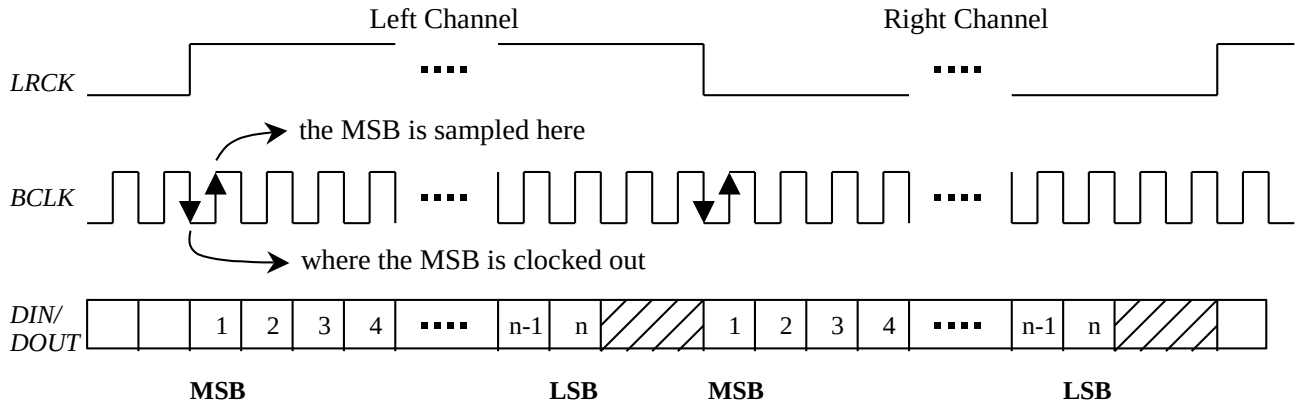


I2S Timing Diagram

For the I²S DAC controller, the audio data is transformed from the parallel format to the serial format before transmission; then the bit data is shifted out one by one with the MSB first via DOUT signal. If the I²S DAC controller is set to 32 bits, at least 32 BCLKs must exist in both the LRCK left and right channels. In the same manner, the audio data is transformed from the coming serial format to the parallel format for an I²S ADC controller.

8.6.1.3 left justified mode

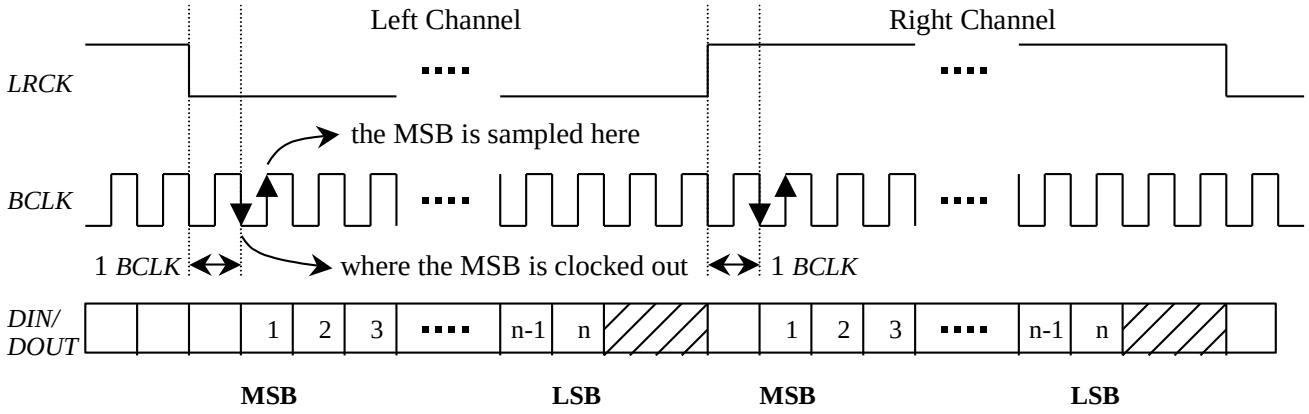
In the I²S DAC controller left-justified mode, the MSB data bit is clocked out at the negative edge of BCLK, which is aligned to the transition of LRCK. The MSB data bit is clocked out by codecs and sampled at the first positive edge of BCLK which follows a LRCK transition. The LRCK is high during left-channel transmission and low during right-channel transmission in the left-justified mode.



I2S Left-Justified Mode Timing Diagram

8.6.1.4 I2S mode

Once the I²S DAC controller is in I²S mode, the MSB data bit is clocked out by the CM6571 at the first negative edge of BCLK which follows a LRCK transition. The MSB data bit is clocked out by codecs and sampled at the second positive edge of BCLK which follows a LRCK transition. LRCK is low during left-channel transmission and high during right-channel transmission in this mode.

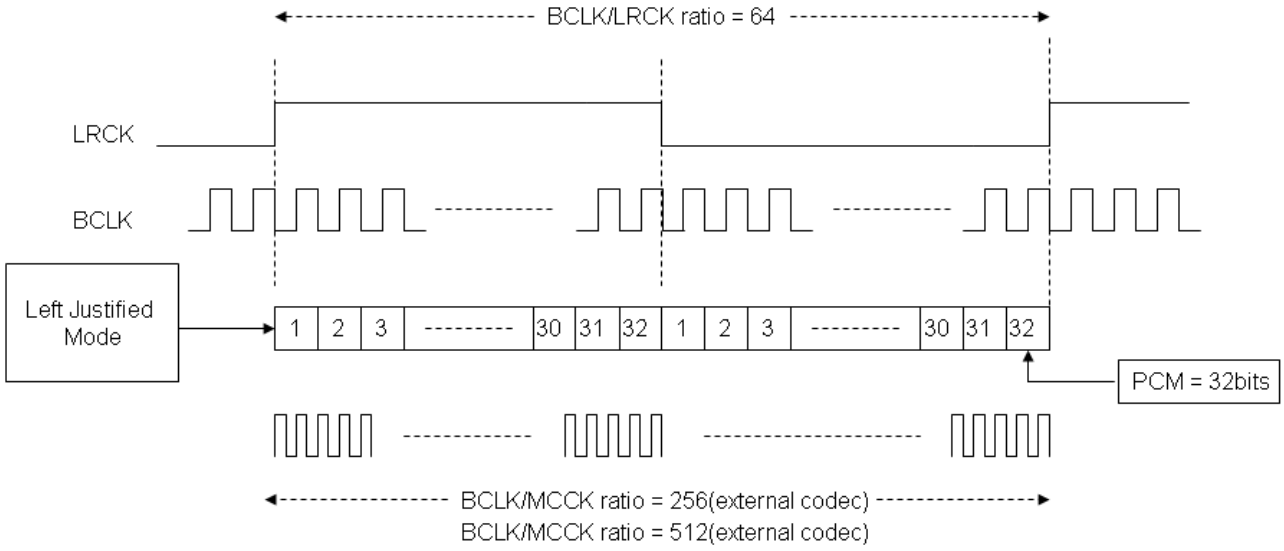


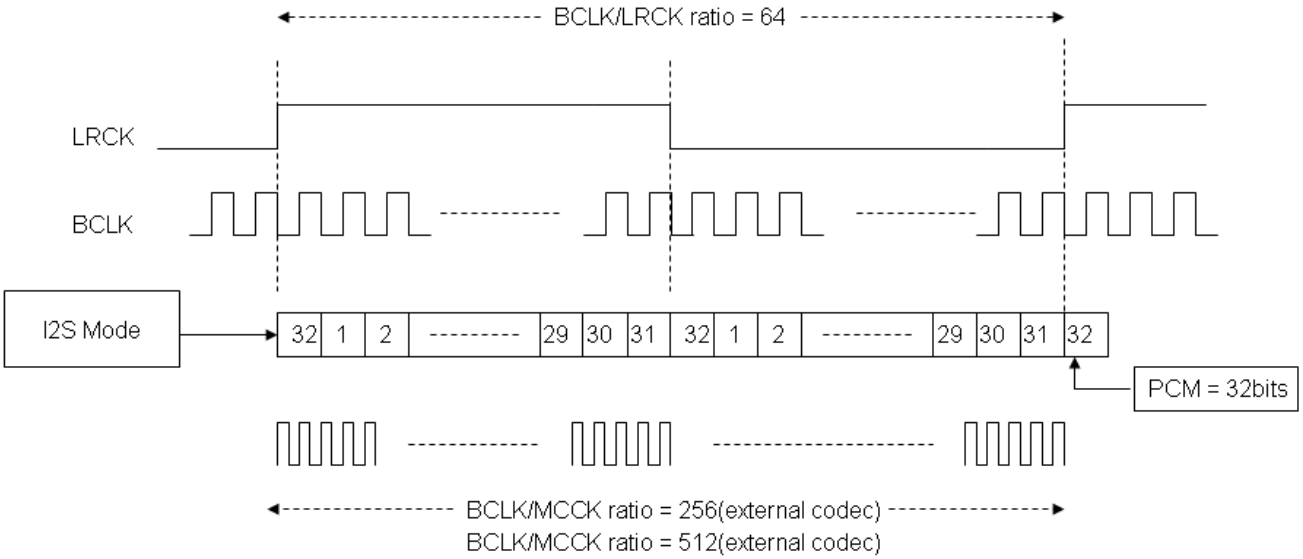
I²S DAC Controller's I²S Mode Diagram

8.6.2 I2S mclk/bclk/lrck ratio and format

Internal Codecs					
	Sampling Freq.	**Resolution**	**Format**	**BCLK/LRCK**	**MCLK/LRCK**
Default		24 bits	Left Justified	64	256
Others	8/11.025/16/ 22.5/32/44.1/48 /88.2/96	16/24 bits	Left Justified/ I2S-Mode	64	256

External Codecs					
	Sampling Freq.	**Resolution**	**Format**	**BCLK/LRCK**	**MCLK/LRCK**
Master mode	8/11.025/16/ 22.5/32/44.1/48	16/24 bits	Left Justified/ I2S-Mode	64	256/512
	88.2/96	16/24 bits	Left Justified/ I2S-Mode	64	256
Slave mode MCLK from CM6523	8/11.025/16/ 22.5/32/44.1/48	16/24 bits	Left Justified/ I2S-Mode	64	256/512
	88.2/96	16/24 bits	Left Justified/ I2S-Mode	64	256
Slave mode MCLK from external	8/11.025/16/ 22.5/32/44.1/48 /88.2/96	16/24 bits	Left Justified/ I2S-Mode	64	128/256/512

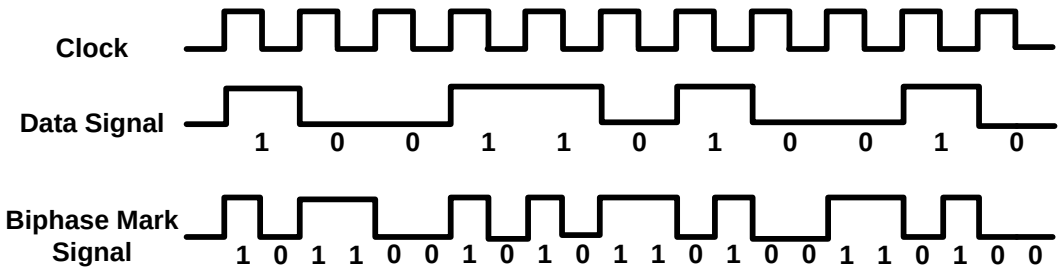




8.7 SPDIF control description

8.7.1 SPDIF frame description

- Audio format: linear 16-bit default, up to 24-bit expandable
- Audio sampling frequencies (Fs):
  - 44.1kHz from CD
  - 48kHz from DAT
  - 32kHz from DSR
- One-way communication: from a transmitter to a receiver
- Control information:
  - V (validity) bit: indicates if audio sample is valid
  - U (user) bit: user free coding, i.e. running time song and track number
  - C (channel status) bit: emphasis, sampling rate and copy permit
  - P (parity) bit: error detection bit to check for good reception
- Coding format: biphase mark except the headers (preambles), for sync purposes
- Bandwidth occupation: 100kHz up to 6Mhz (no DC)
- Signal bitrate is 2.8Mhz (Fs=44.1kHz), 2Mhz (Fs=32kHz) and 3.1Mhz (Fs=48kHz)



SPDIF Biphase Mark Signal Diagram

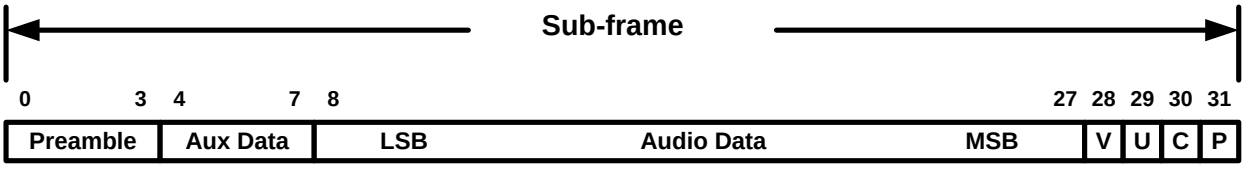
Preamble	Cell Order (last cell "0")	Cell Order (last cell "1")
"B"	11101000	00010111
"M"	11100010	00011101
"W"	11100100	00011011

Preamble B: Marks a word containing data for channel A (left) at the start of the data-block.

Preamble M: Marks a word with data for channel A that is not at the start of the data-block.

Preamble W: Marks a word containing data for channel B (right, for stereo). When using more than two channels, this could also be any other channel (except for A).

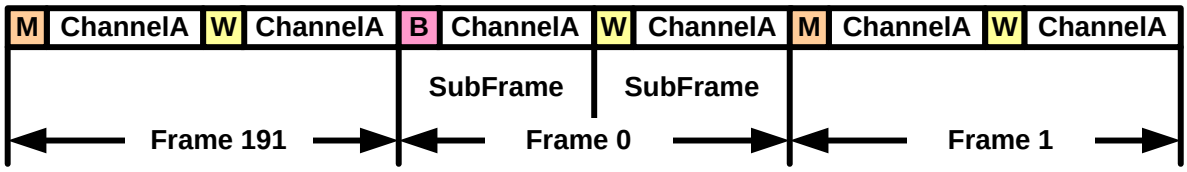
The number of subframes that are used depends on the number of channels that are transmitted. A CD player uses channels A and B (left/right), so each frame contains two subframes. A block contains 192 frames and starts with the preamble B:



V: valid, U: user data, C: channel-status data, P: parity bit

SPDIF Sub-frame Description

In each block, 384 bits of channel status and subcode info are transmitted. The channel-status bits are equal for both subframes, so only 192 useful bits are transmitted:



192-bit SPDIF Frame Preamble Description Diagram

8.7.2 SPDIF out channel status

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Byte 0	**Consumer /Professional**	**Audio/ Non-audio**	**Copyright**	**Pre-emphasis**			**Mode**	
Default	0 (P)	0 (P)	1 (P)	0 (P)	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)
Byte 1	**Category Code**							**L**
Default	0 (P)	0 (P)	0 (P)	0(P)	0 (P)	0 (P)	0 (P)	0 (P)
Byte 2	**source number**				**Channel Number**			
Default	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)
Byte 3	**Sampling Frequency**				**Clock Accuracy**		**Reserved**	
Default	0 (P)	0 (P)	0 (P)	0 (P)	0 (fixed)	0 (fixed)	0 (fixed)	0 (fixed)

Note: P bit can be programmed by USB HID or USB vendor command

9 DSP function description

9.1 Operation modes

It basically supports four operation modes with different power management levels for easy operating control: Power Down/ENC ON/By-Pass/Suspend. It could be controlled by 2 HW mode_selector input pins (MSEL_0,MSEL_1) under default setting, or by I2C command control set from the host controller/baseband. When I2C is chosen to switch these modes, the DSP receives the mode switch command from Baseband chip through I2C interface and writes the result to the two-bit mode_sel registers to handle the mode/power control. If baseband chip choose I2C interface to control the mode selection, then some function blocks will be kept alive at Suspend and Power Down modes.

9.1.1 there are two bits for mode selection:

Mode_Sel Pins [1:0] Register[1:0]	Mode	Description
00	Power Down (default)	Default state for power saving in phone's Standby, Sleep, Deep Sleep, or Power-off states
01	Active (ENC/AEC/NR ON)	Chip and voice processor is turned on for phone active state (calling) (ENC is the default function, host CPU could switch the function to AEC or NR for different applications via I2C commands)
11	By-Pass	By-pass voice processor and redirect Mic-In signals to Mic-Out directly (An option allowing users to turn off ENC/AEC/NR functions during the call or other applications)
10	Suspend	Reserved alternative Suspend mode in phone's Standby or Sleep states especially for keeping new downloaded F/W codes in the internal RAM saving the reloading time for ENC ON

9.2 Mode state diagram and power management

The following graphs are two Mode Switch State Diagrams and corresponding power level (level 0-4) for Mode_Sel and I2C interface respectively:

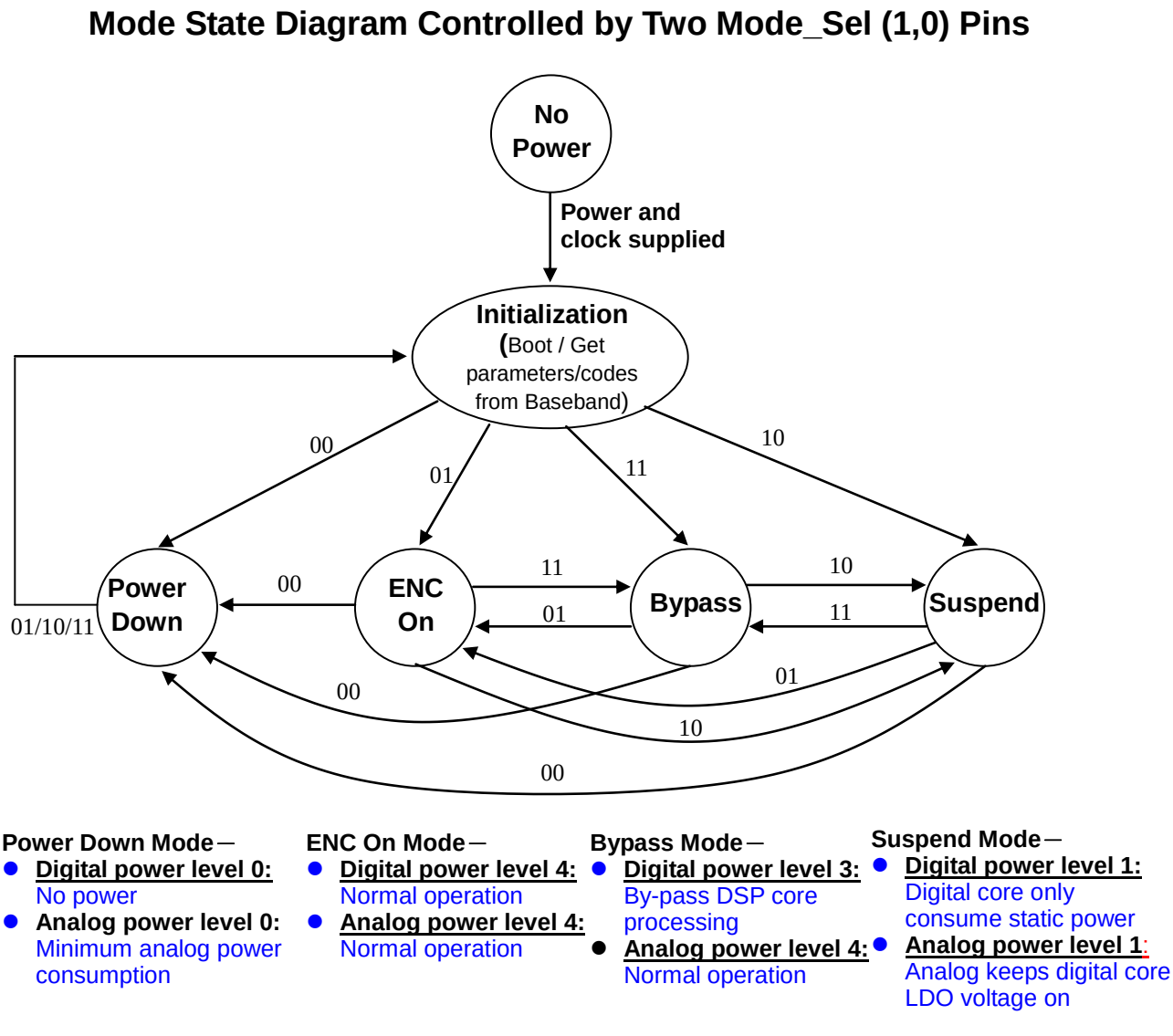
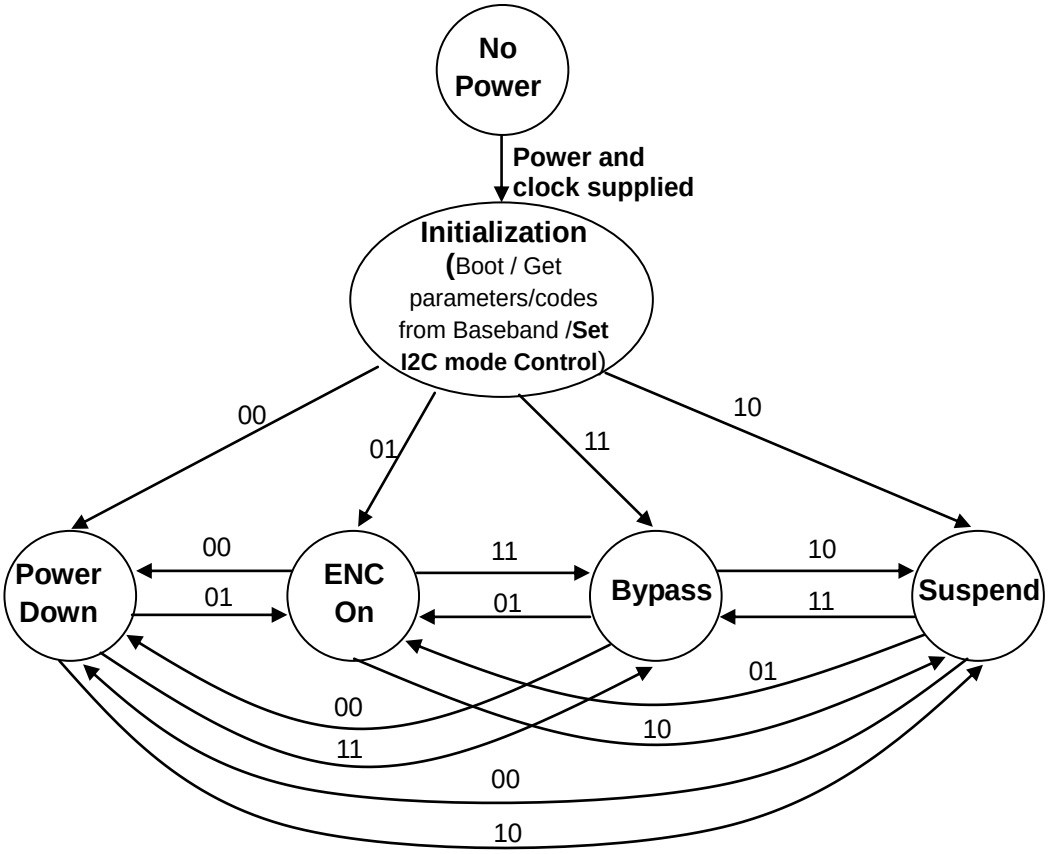


Figure 9.1 Mode State Diagram (by Mode_Sel pins)

Mode State Diagram Controlled by I2C Bus



Power Down Mode—
- **Digital power level 2:** DSP core is operated at a lowest frequency
- **Analog power level 2:** Analog keeps digital core/PLL LDO voltages on

ENC On Mode—
- **Digital power level 4:** Normal operation
- **Analog power level 4:** Normal operation

Bypass Mode—
- **Digital power level 3:** By-pass DSP Core processing
- **Analog power level 4:** Normal operation

Suspend Mode—
- **Digital power level 2:** DSP core is operated at a lowest frequency
- **Analog power level 2:** Analog keeps digital core/PLL LDO voltages on

Figure 9.2 Mode State Diagram (by I2C interface)

9.3 Recommended control methods for DSP core

There are three recommended control scenarios for different customer considerations. These are as follows:

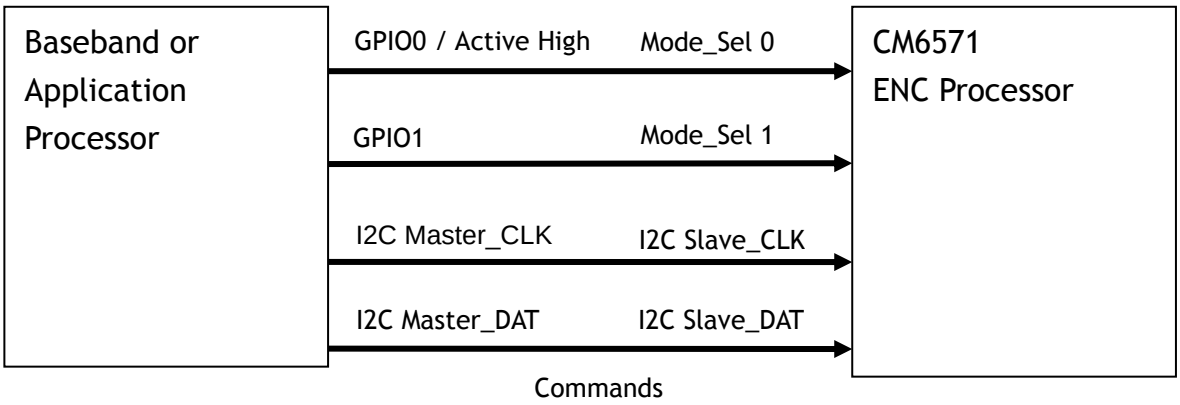
9.3.1 scenario I

Mode_Sel pins control for no custom tuning or just programming parameters with the best power saving

In typical cases, when all default HW settings and DSP algorithm ROM codes could satisfy your needs, or you just need to change some ROM code parameters or set HW registers through I2C interface, we suggest you use Mode_Sel 0/1 pins to simply control chip operation mode for better power saving. In this way, the Power Down mode will go into power level 0 and consume almost no power for Phone Standby/Sleep/Deep Sleep or Power-Off status. When phone is active during a call, switch to ENC mode by baseband's active signal pin or a GPIO pin (drive high) to Mode_Sel0 pin. Pull it low back to Power Down when ending a call to Standby status. Another GPIO pin could drive Mode_Sel1 pin high (while Mode_Sel 0 is high at the same time) to enter By-Pass mode when you choose to turn off ENC function or when the design does not use CM6571's AEC or NR functions in speakerphone and recorder applications. The phone status should match the following operation modes:

Phone Status	Power-Off	Stand-By/Sleep/Deep Sleep	Active (Effect On)	Active (Effect Off)
Operation Mode	Power Down (No power supply)	Power Down	Active (ENC ON, or AEC or NR by I2C command)	By-Pass
Mode_Sel0/1 Control	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=1

In this scenario, note that the baseband needs to program the parameters or HW registers through I2C every time before entering into Phone Active/Calling status with ENC chip working (very short time~0.12ms).

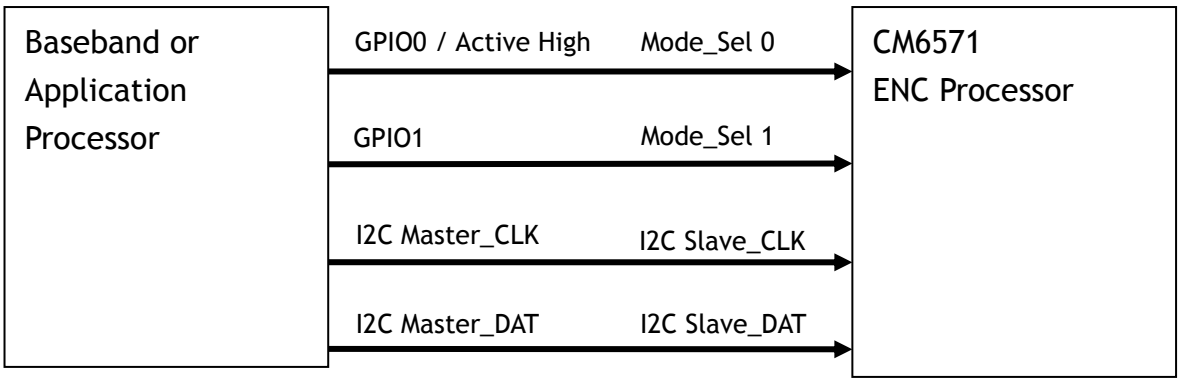


9.3.2 scenario II

Mode_Sel pins control for demand to download firmware codes with power saving

When default DSP algorithm ROM codes could NOT satisfy your needs, CM6571 ENC chip allows baseband to download a whole new version of codes into the RAM program through I2C interface. In this situation, we suggest you still use Mode_Sel 0/1 pins to simply control chip operation mode for better power saving. However, to avoid downloading time (1.16sec for 32Kbytes FW @ I2C fast mode) every time getting start from Power Down mode, it might be necessary to use Suspend mode (Mode_Sel0=low, Mode_Sel1=high) for Phone Standby or Sleep status, which will keep the RAM program/data alive. When phone is active during a call, switch to active ENC ON mode by baseband's phone active signal pin or a GPIO pin to pull-high Mode_Sel0 pin, and Mode_Sel1 pin must be pull low at the same time. Reverse back to suspend when ending a call to Standby/Sleep status. The same as Scenario I, drive both Mode_Sel 0/1 pins to high at the same time to enter By-Pass mode when you want to turn off ENC in a call. The phone status should match the following operation modes:

Phone Status	Power-Off/ Deep Sleep	Stand-By/Sleep	Active (Effect On)	Active (Effect Off)
Operation Mode	Power Down (or No power supply)	Suspend	Active (ENC ON, or AEC or NR by I2C command)	By-Pass
Mode_Sel0/1 Control	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=0 Mode_Sel 1=1	Mode_Sel 0=1 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=1



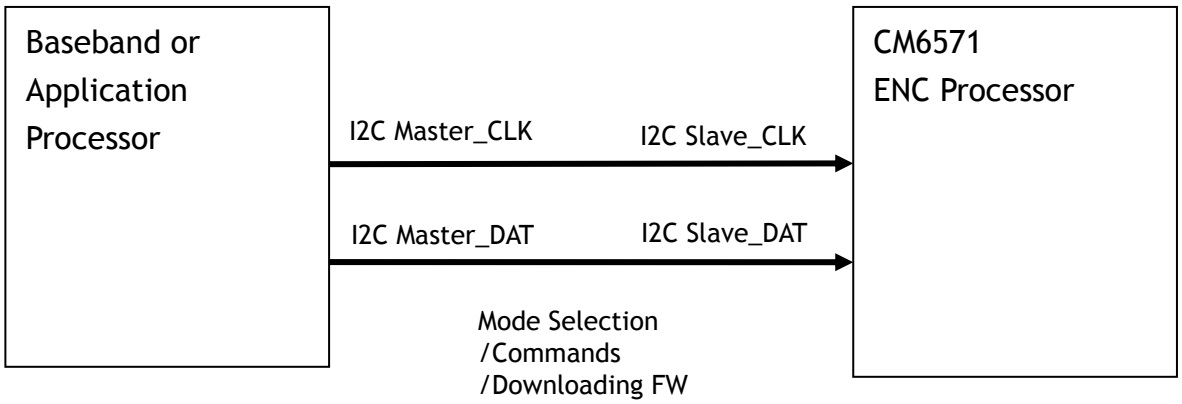
Downloading FW

9.3.3 scenario III

I2C control only for convenience

CM6571 ENC chip also allows baseband to switch the operation modes via I2C programming hardware registers if customers do not want to use additional GPIO control. This way only uses I2C for all control over ENC chip but will need higher power levels to keep I2C slave interface and digital core alive in Standby status. In this situation, we suggest to keep Power Down (00) or Suspend (10) mode for Phone Standby status (in this I2C control scenario, two modes are actually the same operation), which will keep the RAM program/data and I2C alive. Therefore, baseband does not need to program or download codes every time when phone is going to Active status for calling. Set registers [1:0] to 01 for ENC ON operation in active normal handset calling. Reverse back to Power Down/Suspend mode when ending a call to Standby/Sleep status. The same with Scenario I and II, set register [1:0] as 11 to enter By-Pass mode when the user (or design) would like to turn off ENC in a call or other applications. The phone status should match the following operation modes via I2C interface writing from the baseband:

Phone Status	Power-Off	Stand-By/Sleep/ Deep Sleep	Active (Effect On)	Active (Effect Off)
Operation Mode	Power Down (No power supply)	Power Down or Suspend	Active (ENC ON, or AEC or NR by I2C command)	By-Pass
Mode_Sel0/1 Control	Mode_Sel 0=0 Mode_Sel 1=0	Mode_Sel 0=0 Mode_Sel 1=0 or 1	Mode_Sel 0=1 Mode_Sel 1=0	Mode_Sel 0=1 Mode_Sel 1=1



9.4 Power level description table of DSP

9.4.1 power levels of DSP core

Power Levels	Digital description	Analog description
0	1.2V core power: **OFF** PLL clock: **OFF** **(No power consumption)**	Analog Logic Power: **ON** Others: **OFF** **Self regulator: 0uA** **External DVDD: 1uA**
1	1.2V core power: **ON** PLL clock: **OFF** Only consume static power (**120uW or 100uA**)	1.2V regulator: **ON** PLL power: **OFF** Others: **OFF** **80uA**
2	1.2V core power: **ON** PLL clock: **ON** DSP and I2C is operated at the lowest frequency 3.792 MHz (**703uW or 585uA**)	1.2V regulator: **ON** PLL power: **ON** Others: **OFF** **80+500uA**
3	1.2V core power: **ON** PLL clock: **ON** ADC digital filter DSP, I2C, and ADDA (in order to avoid pop-noise) is operated at the lowest frequency 3.792 MHz (**772uW or 643uA**)	1.2V/PLL: **ON** ADC/DAC: **OFF** Mic Bias/ OPA of DAC: **ON** **1050+500uA**
4	1.2V core power: **ON** PLL clock: **ON** ENC normal operation mode. DSP is operated at 45.5 MHz (**17mW or 14.2mA**)	1.2V regulator: **ON** PLL power: **ON** Others: **ON** **4200+500uA**

Phone state and CM6571 state contrast table

Phone States	CM6571 States
Active	**ENC ON or Bypass**
Stand-by	**Suspend**
Switch-Off	**Power Down**
Power-Off	**No power**

10 Electrical characteristics

10.1 Absolute maximum ratings

Test conditions: DV50 = 5V, AV50 = 5V, DGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Storge temperature	T_S	-25	-	150	°C
Operating ambient temperature	T_A	0	25	75	°C
Digital supply voltage(DV50)		4.5	5.0	5.5	V
Analog supply voltage(AV50)		4.5	5.0	5.5	V
Digital supply voltage2(DVDD)		1.75	1.8/2.8	3.6	V
Analog supply voltage2(AVDD)		2.2	2.8	3.6	V
I/O pin voltage	-	GND	-	3.3	V
ESD (Body mode)			±4000		V
ESD (Machine mode)			±200		V

10.2 Recommended operation conditions

Parameter	Symbol	Min.	Typ	Max.	Units
Digital supply voltage(DV50)	-		5		V
Analog supply voltage(AV50)			5		V
Digital supply voltage2(DVDD)		1.75	1.8/2.8	3.6	V
Analog supply voltage2(AVDD)		2.4	2.8	3.6	V
Operating ambient temperature			25		°C
Crystal clock	-		12.000		MHz

10.3 Power consumption

Test Conditions: DV50=5V, AV50 = 5V, DGND =0V, TA=+25°C
Sample Rate=48kHz, 16Bits, Operation: HP-Out Playback+Mic-In Recording, EQ disable, Spdif out disable

Parameter	Symbol	Min.	Typ	Max.	Units
Total power consumption (Playback + Record)	-	-	76	-	mA
Standby power consumption	-	-	58	-	mA
Suspend mode power consumption	-	-	1650	-	uA

10.4 DC characteristics

Test Conditions: DV50=5V, V_{DD} = 3.3V, DGND =0V, TA=+25°C, V_{DD} = 3.3V

Parameter	Symbol	Min.	Typ	Max.	Units
Input voltage range	Vin	DGND-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage range	Vout	0	-	V_{DD}	V
High-level input voltage	Vih	0.7V_{DD}	-	-	V
Low-level input voltage	Vil	-	-	0.3V_{DD}	V
High-level output voltage	Voh	2.4	-	-	V
Low-level output voltage	Vol		-	0.4	V
Input leakage current	Iil	-10	-	10	uA
Output leakage current	Iol	-10	-	10	uA
Output buffer driver current	-	2	8	16	mA
SPDIF transmit output driver current	-	2	8	16	mA

10.5 Audio performance

10.5.1 DAC audio quality

TA=25℃, DV50=5V, AV50=5V

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full-scale Output Voltage	10KΩ loading fs=48kHz		0.95		Vrms
	32Ω loading fs=48kHz		0.82		Vrms
THD+N @ Vout=-3dB	10KΩ loading fs=48kHz/16bits,A-Weighted	-78	-82dB	-93	dB
	10KΩ loading fs=96kHz/24bits, A-Weighted	-79	-82dB	-94	dB
	32Ω loading fs=48kHz/16bits,A-Weighted	-67	-82dB	-92	dB
	32Ω loading fs=96kHz/24bits,A-Weighted	-67	-82dB	-95	dB
Dynamic Range with Signal Present	10KΩ loading fs=48kHz/16bits,A-Weighted		91		dB
	10KΩ loading fs=96kHz/24bits, A-Weighted		94		dB
	32Ω loading fs=48kHz/16bits,A-Weighted		92		dB
	32Ω loading fs=96kHz/24bits,A-Weighted		94		dB
Noise Level during System Activity	10KΩ loading fs=48kHz/16bits,A-Weighted		94		dB
	10KΩ loading fs=96kHz/24bits, A-Weighted		96		dB
	32Ω loading fs=48kHz/16bits,A-Weighted		96		dB
	32Ω loading fs=96kHz/24bits,A-Weighted		94		dB
Inter-Channel Phase Delay	100Hz ~ 20kHz	+0.02		+1.05	Deg
Sampling Frequency Accuracy	10KΩ loading fs=48kHz/16bits,A-Weighted	-0.0043		+0.0015	%

Channel Separation		10KΩ loading fs=48kHz/16bits,A-Weighted	98	108	119	dB
		32Ω loading fs=48kHz/16bits,A-Weighted	67	72	78	dB
Magnitude Response	Frequency Response	10KΩ loading fs=48kHz/16bits,A-Weighted	-0.085		-0.937	dB
	Passband Ripple	10KΩ loading fs=48kHz/16bits,A-Weighted			0.291	dB

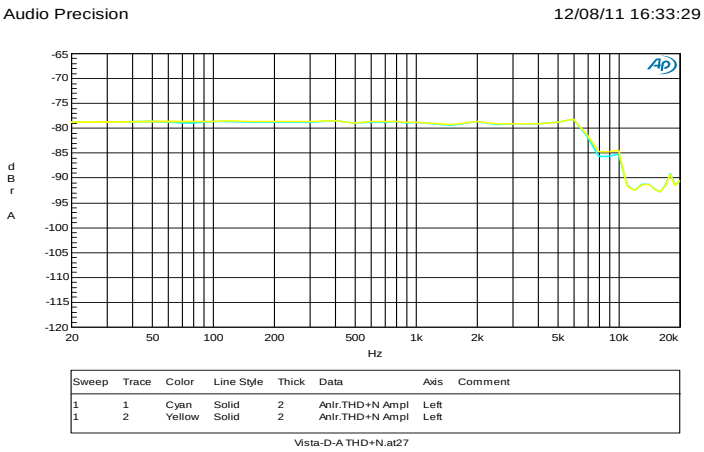


FIGURE 1. 48K/16BIT, 10K LOADING DAC, THD+N

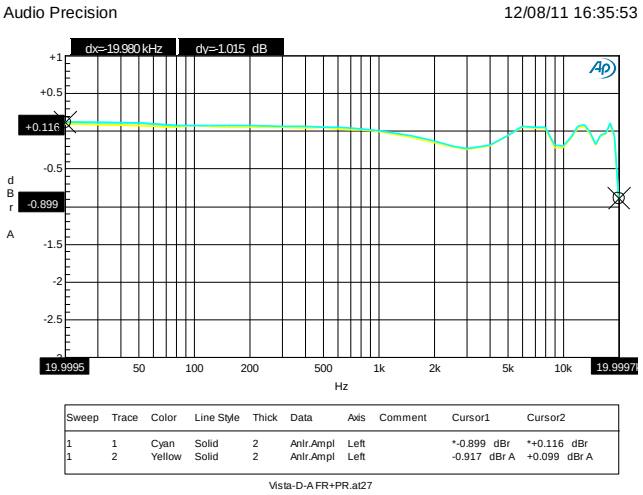


FIGURE 2. 48K/16BIT, 10K LOADING DAC, FREQUENCY RESPONSE

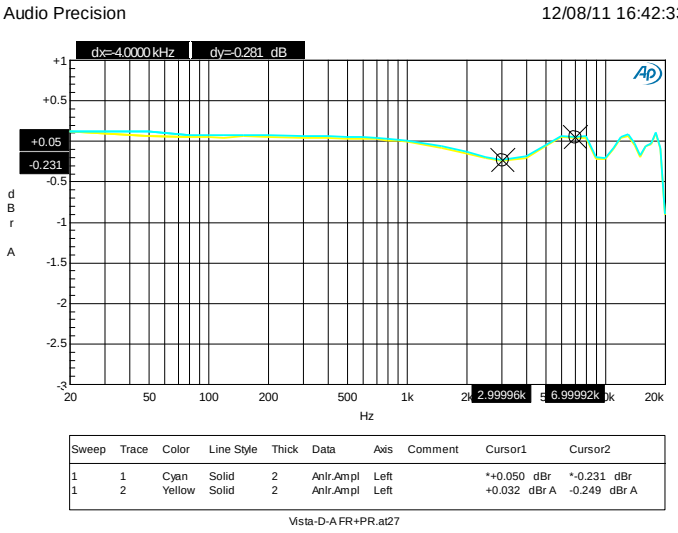


FIGURE 3. 48K/16BIT, 10K LOADING DAC, PASSBAND RIPPLE

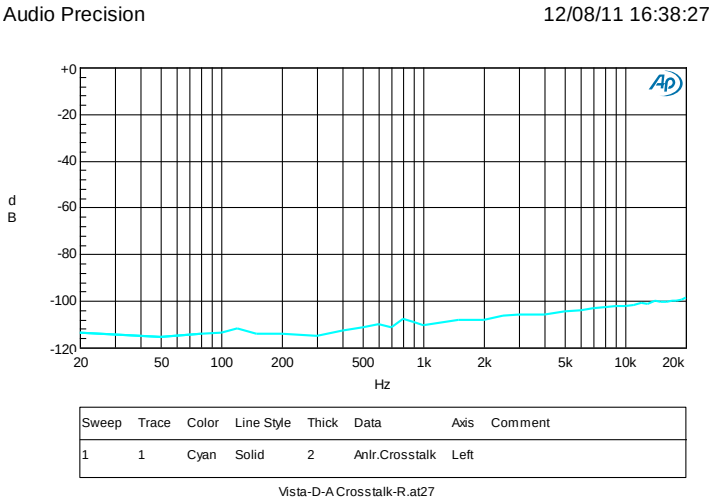


FIGURE 4. 48K/16BIT, 10K LOADING DAC, CROSSTALK L

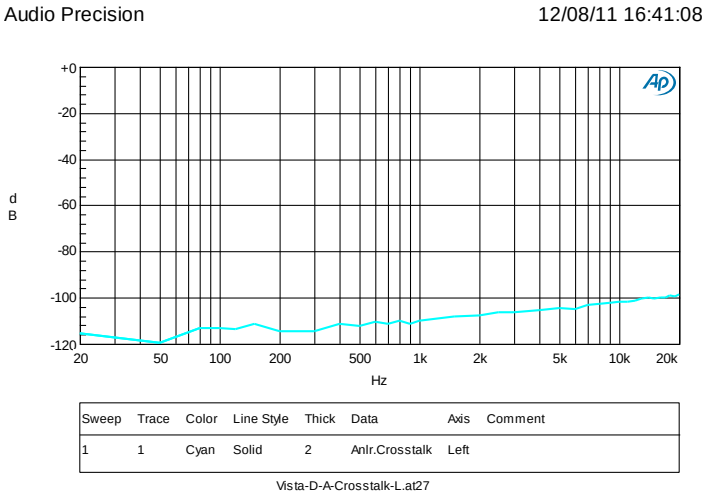


FIGURE 5. 48K/16BIT, 10K LOADING DAC, CROSSTALK R

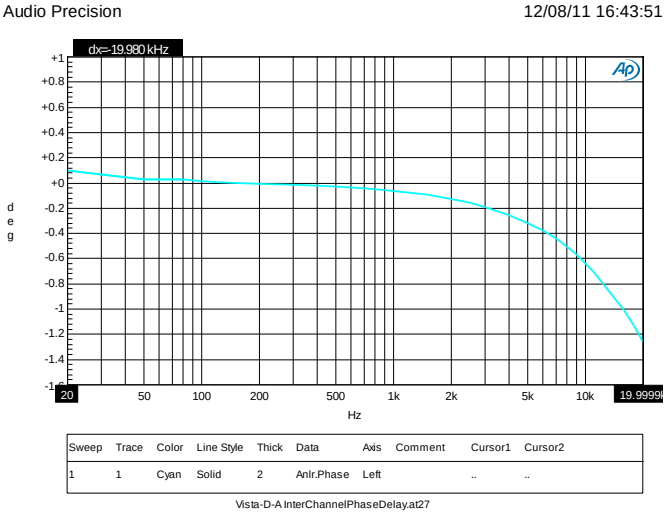


FIGURE 6. 48K/16BIT, 10K LOADING DAC, PHASE DELAY

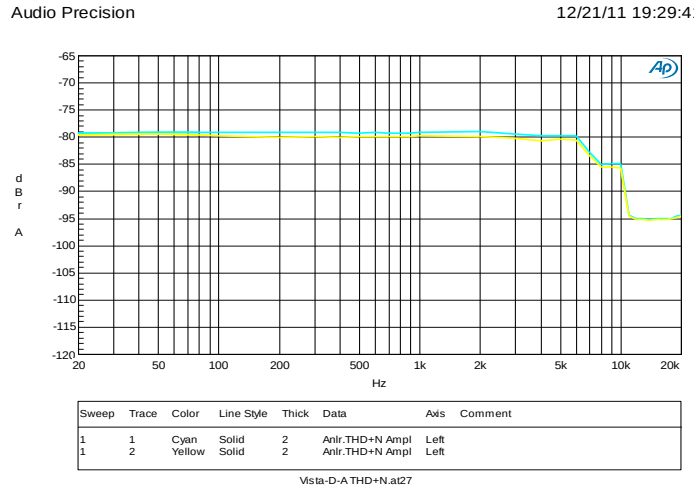


FIGURE 7. 96K/24BIT, 10K LOADING DAC, THD+N

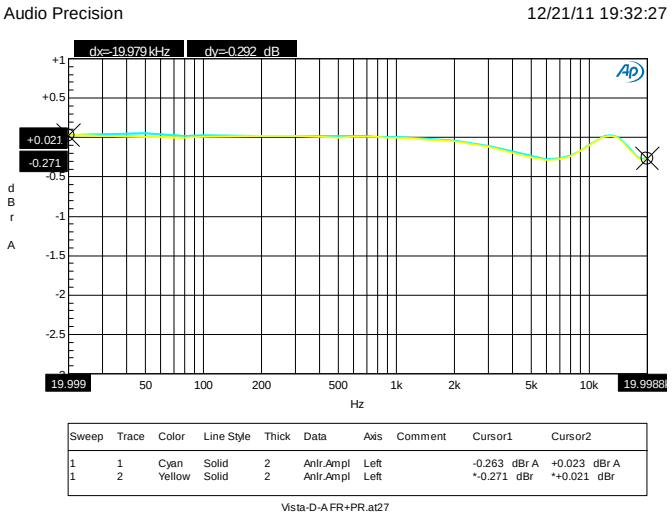
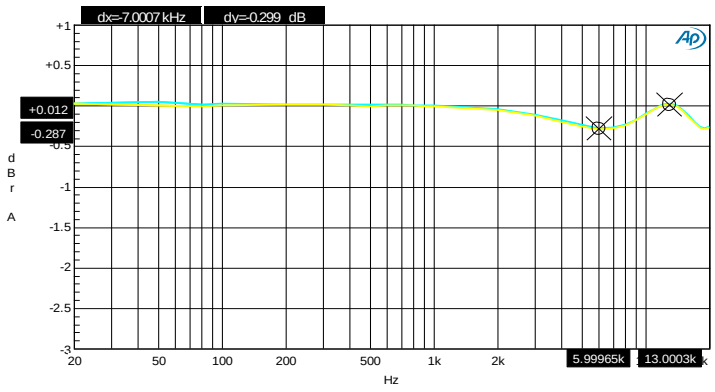


FIGURE 8. 96K/24BIT, 10K LOADING DAC, FREQUENCY RESPONSE

Audio Precision 12/21/11 19:32:27

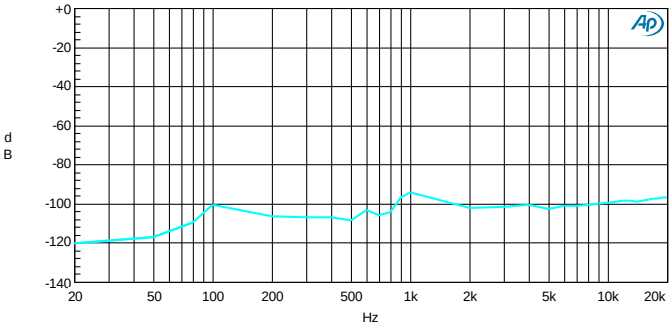


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	2	Anlr.Ampl	Left		+0.022 dBr A	-0.277 dBr A
1	2	Yellow	Solid	2	Anlr.Ampl	Left		*+0.012 dBr	*-0.287 dBr

Vista-D-A FR+PR.at27

FIGURE 9. 96K/24BIT, 10K LOADING DAC, PASSBAND RIPPLE

Audio Precision 12/21/11 19:38:25

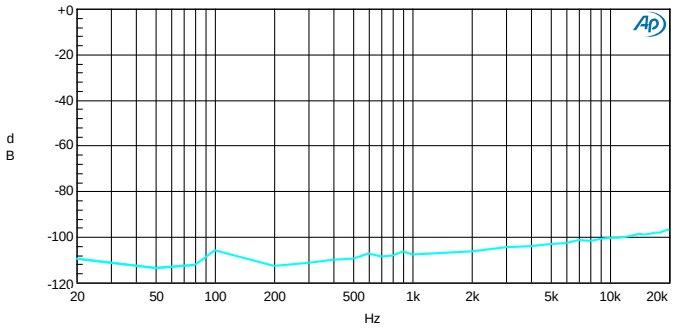


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.Crosstalk	Left	

Vista-D-A-Crosstalk-L.at27

FIGURE 10. 96K/24BIT, 10K LOADING DAC, CROSSTALK L

Audio Precision 12/21/11 19:36:13

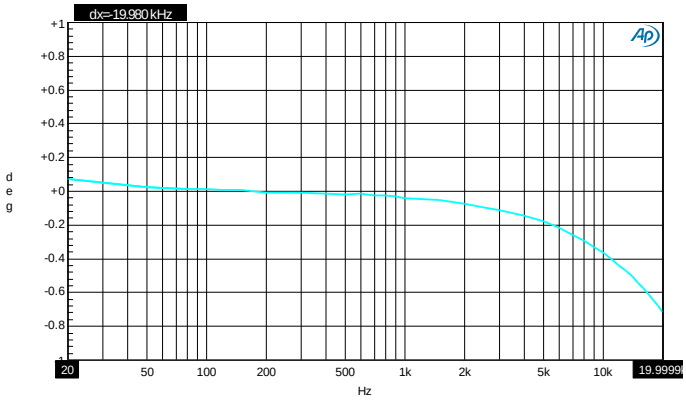


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.Crosstalk	Left	

Vista-D-A Crosstalk-R.at27

FIGURE 11. 96K/24BIT, 10K LOADING DAC, CROSSTALK R

Audio Precision 12/21/11 19:40:48



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	2	Anlr.Phase	Left		..	..

Vista-D-A InterChannelPhaseDelay.at27

FIGURE 12. 96K/24BIT, 10K LOADING DAC, PHASE DELAY

10.5.2 ADC audio quality

TA=25℃, DV50=5V, AV50=5V, input test signal is 997Hz sine wave, measure bandwidth is 20Hz to 20kHz

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full-scale Output Voltage	Microphone fs=48kHz		1.11		Vrms
	Line in fs=48kHz		1.08		
THD+N @ Vout=-3dB	Microphone fs=48kHz/16bits,A-Weighted	-81	-82	-89	dB
	Microphone fs=96kHz/24bits, A-Weighted	--82	-82	-91	dB
	Line in fs=48kHz/16bits,A-Weighted	-82	-82	-90	dB
	Line in fs=96kHz/24bits,A-Weighted	-82	-82	-90	dB
Dynamic Range with Signal Present	Microphone fs=48kHz/16bits,A-Weighted		90		dB
	Microphone fs=96kHz/24bits, A-Weighted		91		dB
	Line in fs=48kHz/16bits,A-Weighted		90		dB
	Line in fs=96kHz/24bits,A-Weighted		90		dB
Sampling Frequency Accuracy	Microphone fs=48kHz/16bits	+0.0001		+0.009	%
	Line in fs=48kHz/16bits	-0.0048		-0.0034	
Channel Separation	Microphone fs=48kHz/16bits	81	86	91	dB
	Microphone fs=96kHz/24bits	83	86	91	dB
	Line in fs=48kHz/16bits	86	86	89	
	Line in fs=96kHz/24bits	87	86	90	
Frequency Response	Microphone fs=48kHz/16bits,A-Weighted	-0.433		-0.484	dB

	Line in fs=48kHz/16bits,A-Weighted	-0.313		-0.695	
Passband Ripple	Microphone fs=48kHz/16bits,A-Weighted			0.204	dB
	Line in fs=48kHz/16bits,A-Weighted			0.159	

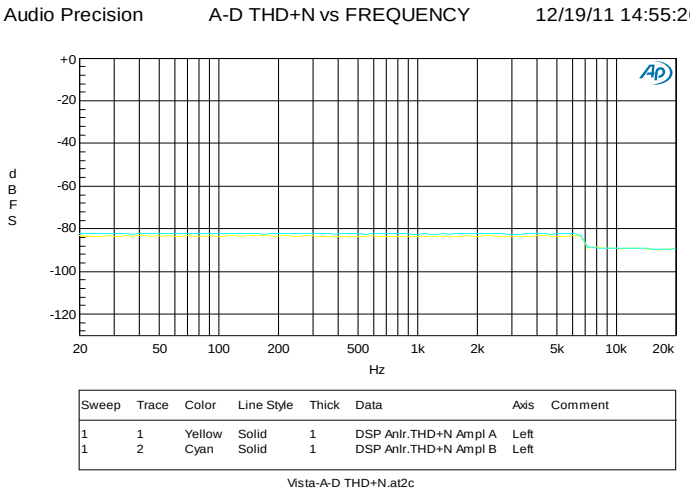


FIGURE 13. 48K/16BIT, MICROPHONE IN, THD+N

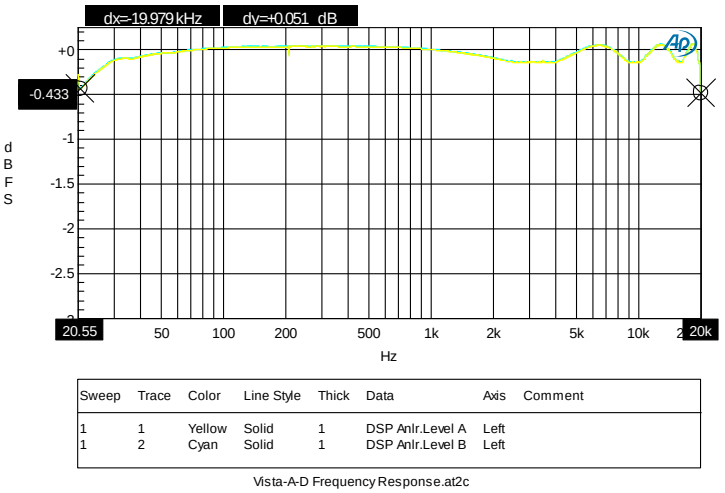
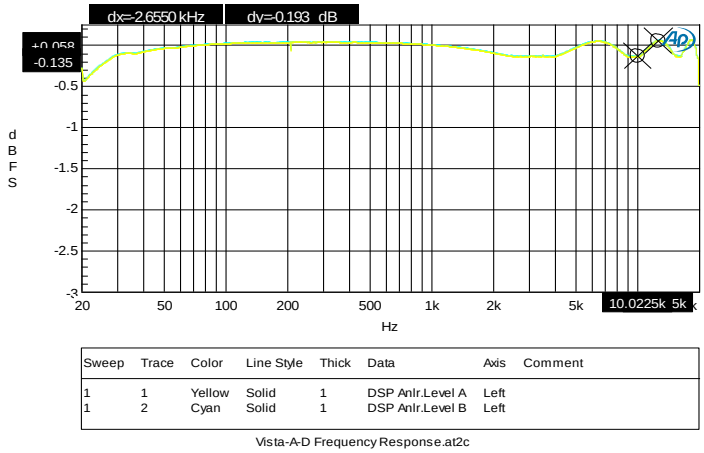


FIGURE 14. 48K/16BIT, MICROPHONE IN, FREQUENCY RESPONSE



5.2.1.1 PASSBAND RIPPLE 48K

FIGURE 15. 48K/16BIT, MICROPHONE IN, PASSBAND RIPPLE

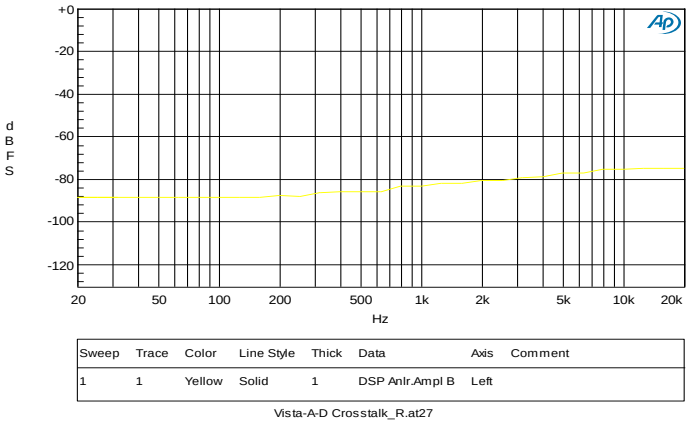


FIGURE 16. 48K/16BIT, MICROPHONE IN, CHANNEL SEPARATION R

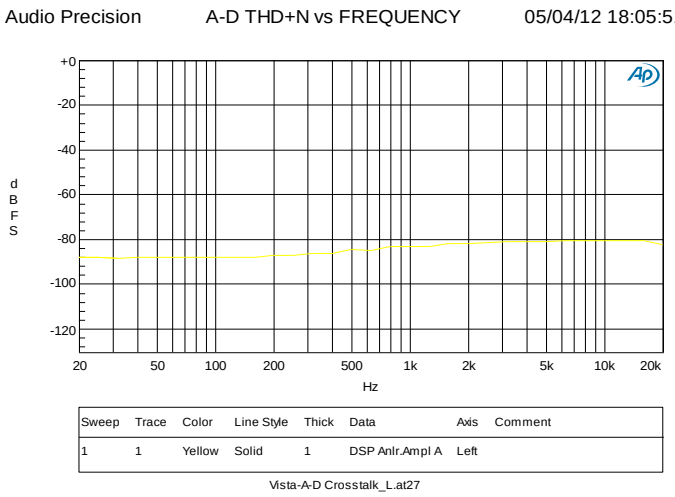


FIGURE 17. 48K/16BIT, MICROPHONE IN, CHANNEL SEPARATION L

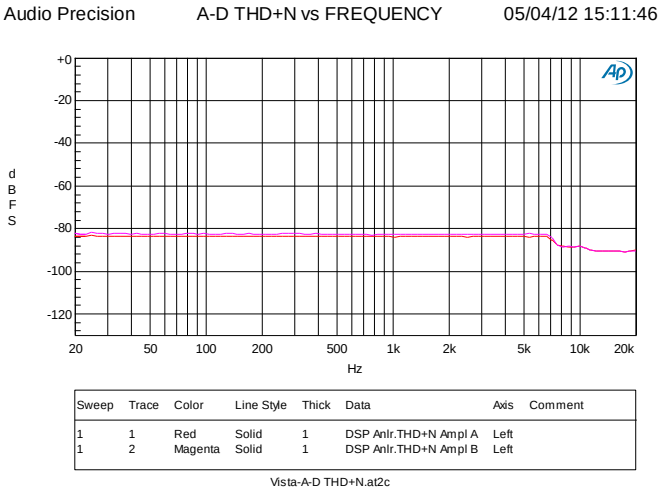


FIGURE 18. 48K/16BIT, LINE IN, THD+N

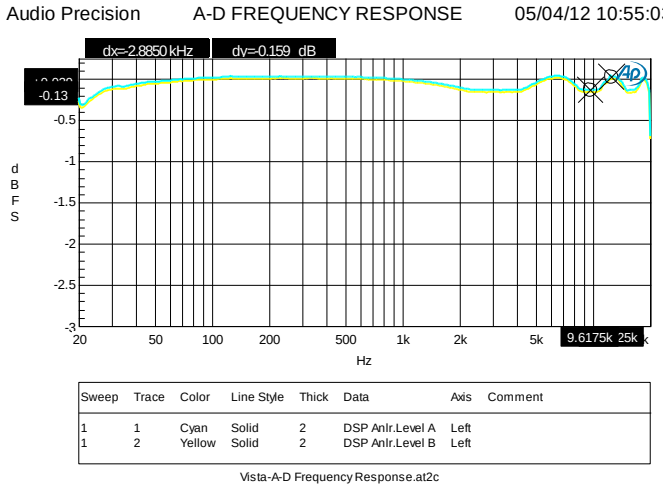


FIGURE 19. 48K/16BIT, LINE IN, PASSBAND RIPPLE

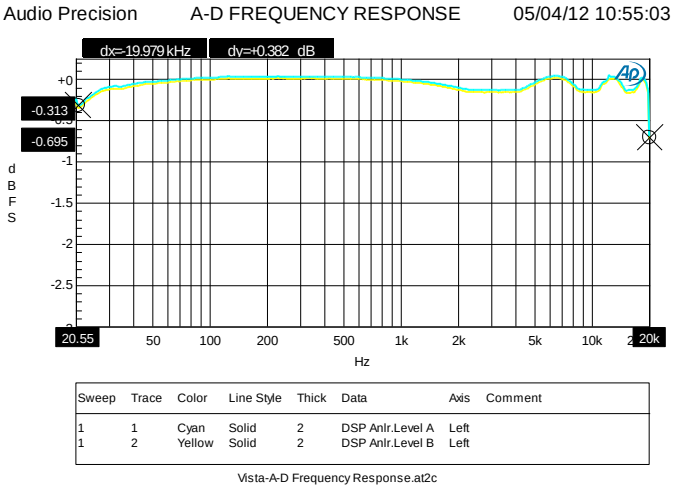


FIGURE 20. 48K/16BIT, LINE IN, FREQUENCY RESPONSE

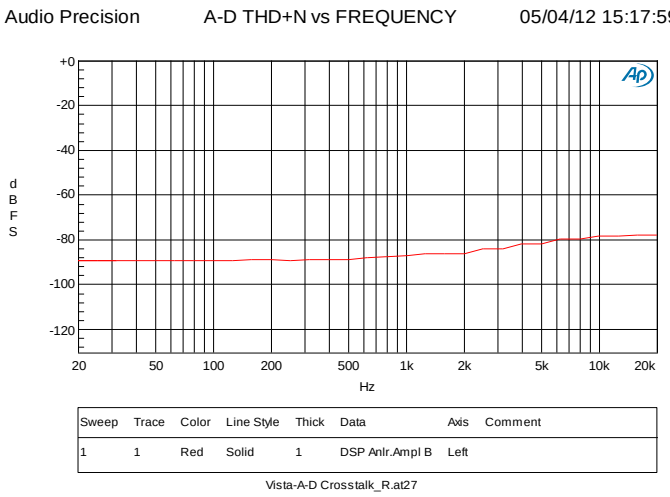


FIGURE 21. 48K/16BIT, LINE IN, CHANNEL SEPARATION R

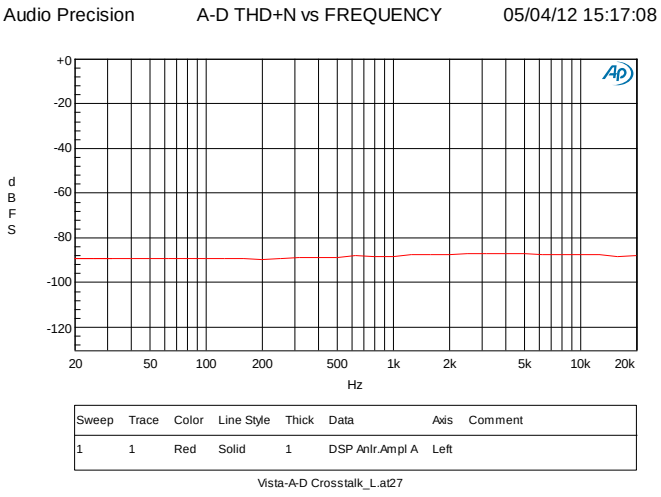


FIGURE 22. 48K/16BIT, LINE IN, CHANNEL SEPARATION L

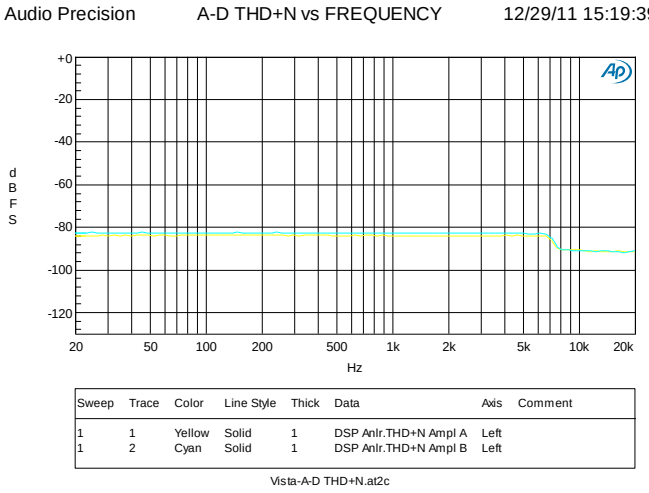


FIGURE 23. 96K/24BIT, MICROPHONE IN, THD+N

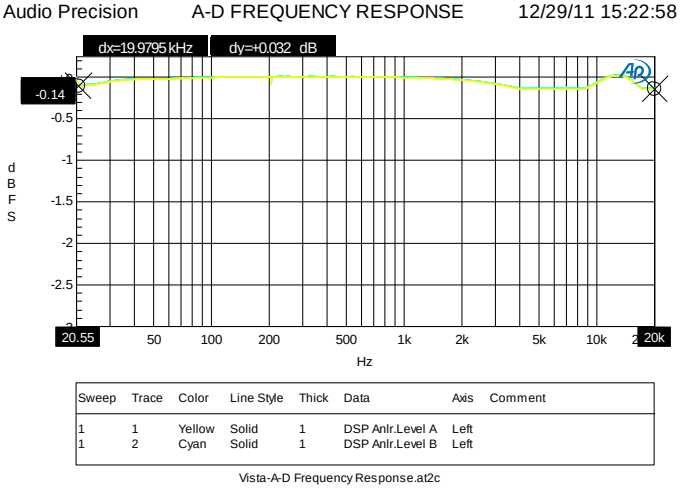


FIGURE 24. 96K/24BIT, MICROPHONE IN, FREQUENCY RESPONSE

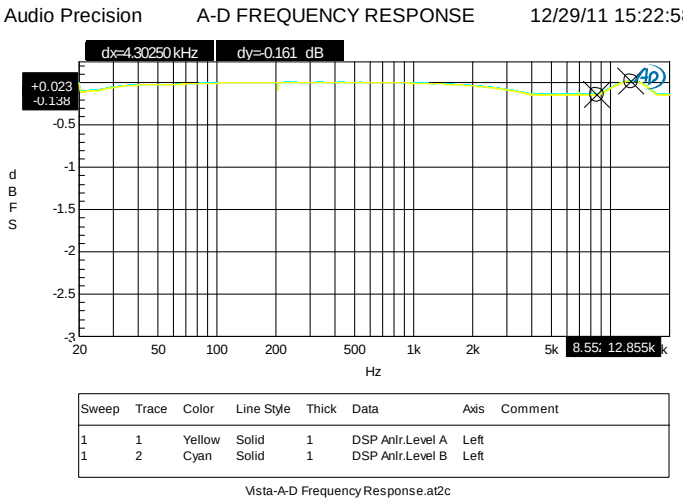


FIGURE 25. 96K/24BIT, MICROPHONE IN, PASSBAND RIPPLE

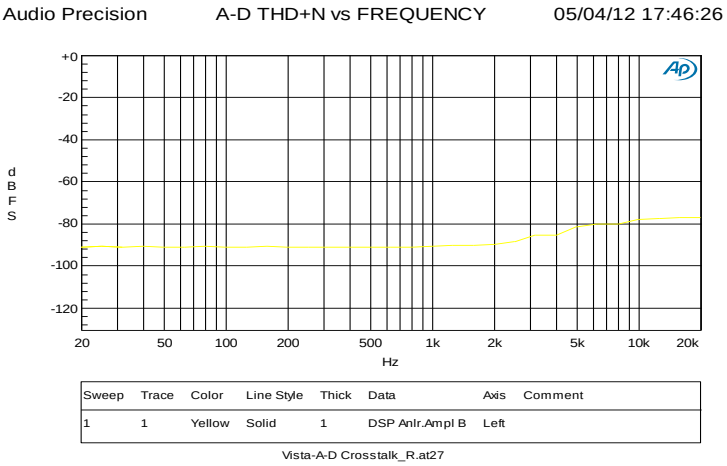


FIGURE 26. 96K/24BIT, MICROPHONE IN, CHANNEL SEPARATION R

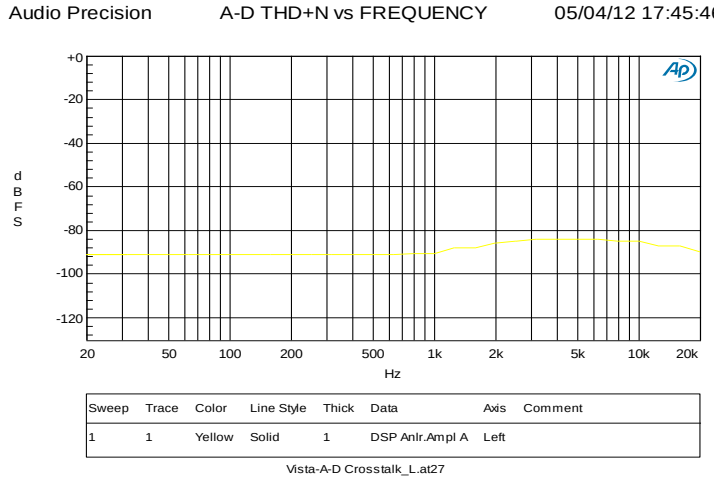


FIGURE 27. 96K/24BIT, MICROPHONE IN, CHANNEL SEPARATION L

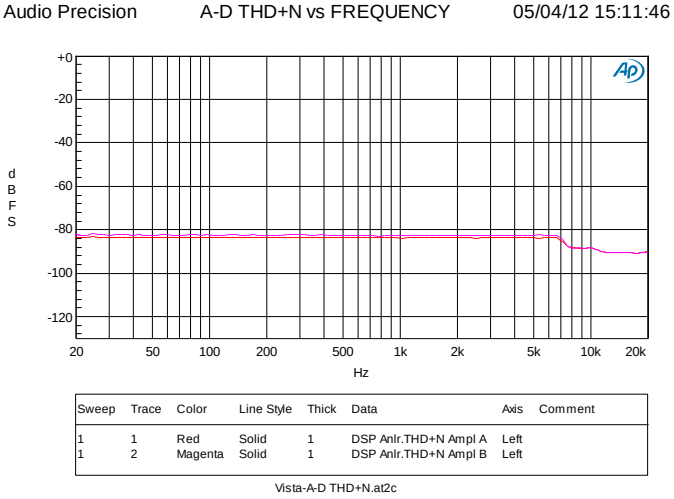


FIGURE 28. 96K/24BIT, LINE IN, THD+N

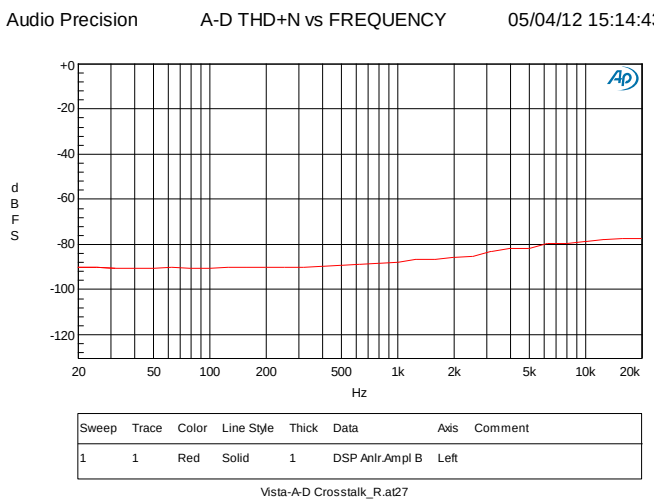


FIGURE 29. 96K/24BIT, LINE IN, CHANNEL SEPARATION R

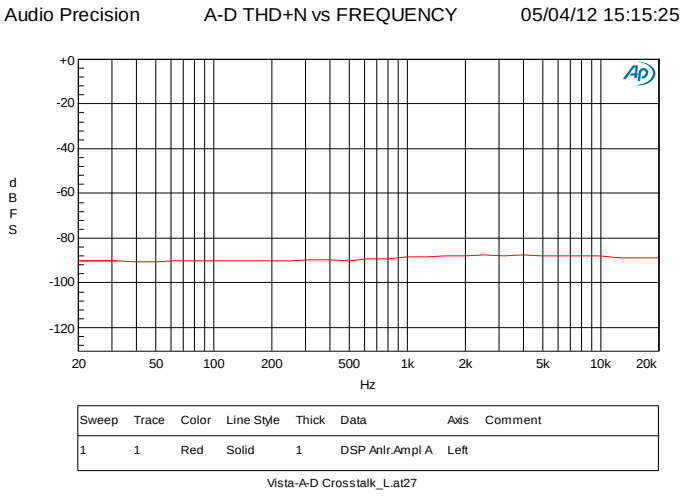


FIGURE 30. 96K/24BIT, LINE IN, CHANNEL SEPARATION L

10.5.3 A-A path audio quality

TA=25℃, DV50=5V, AV50=5V

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full-scale Output Voltage	Microphone to Line out		1.09		Vrms
THD+N @ Vout=-3dB	Microphone to Line out fs=48kHz/16bits,A-Weighted	-80	-80	-81	dB
Dynamic Range with Signal Present	Microphone to Line out fs=48kHz/16bits,A-Weighted		92		dB
Channel Separation	Microphone to Line out fs=48kHz/16bits,A-Weighted	74	104	119	dB
Frequency Response	Microphone to Line out fs=48kHz/16bits,A-Weighted	-0.194		+0.484	dB
Passband Ripple	Microphone fs=48kHz/16bits,A-Weighted			0.1	dB

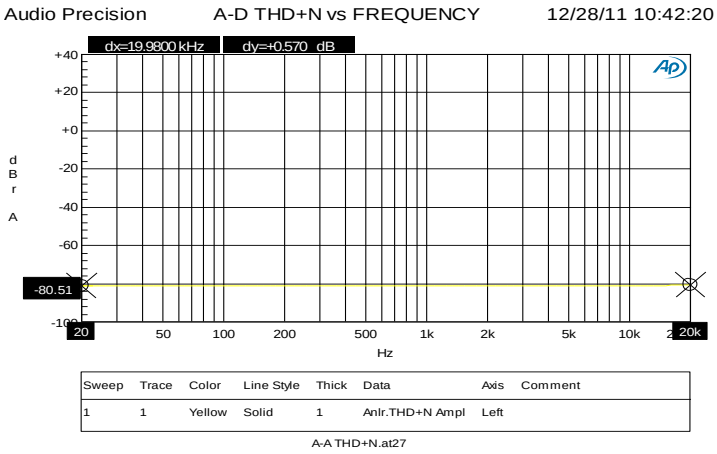


FIGURE 31. LINE IN TO LINE OUT, THD+N

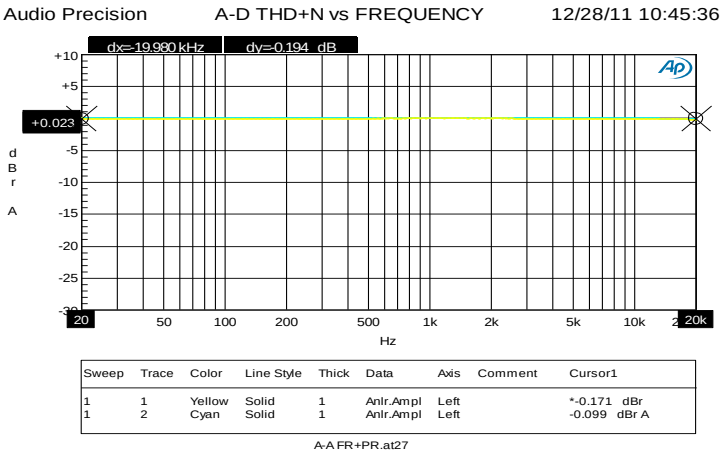


FIGURE 32. LINE IN TO LINE OUT, FREQUENCY RESPONSE

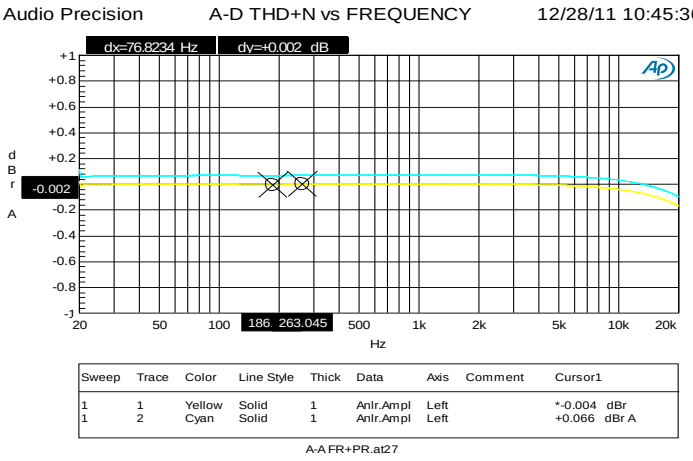


FIGURE 33. LINE IN TO LINE OUT, PASSBAND RIPPLE

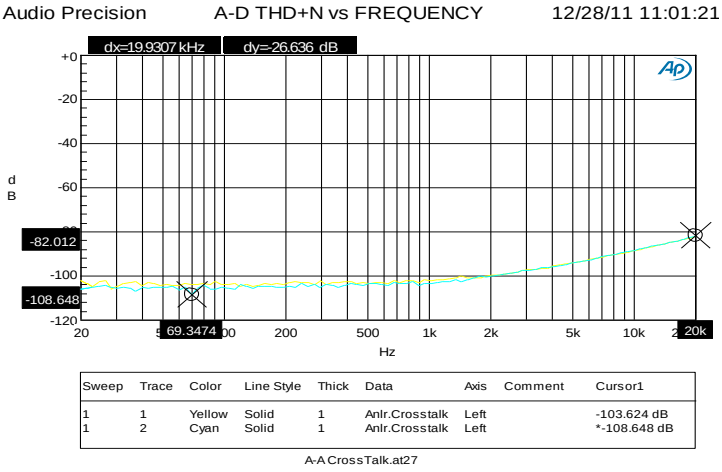


FIGURE 34. LINE IN TO LINE OUT, CROSSTALK L

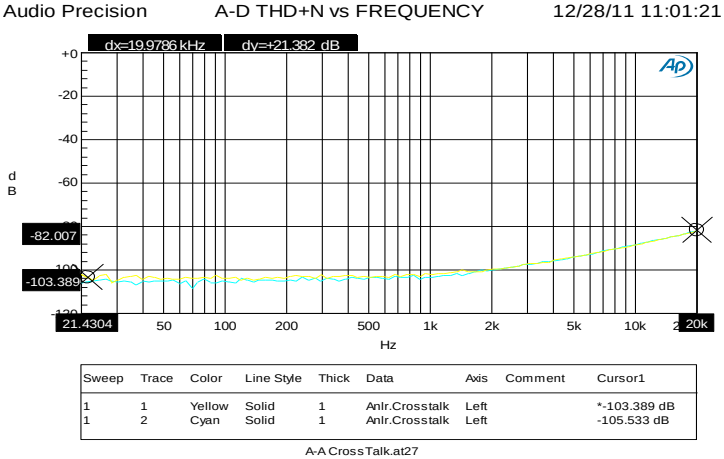


FIGURE 35. LINE IN TO LINE OUT, CROSSTALK R

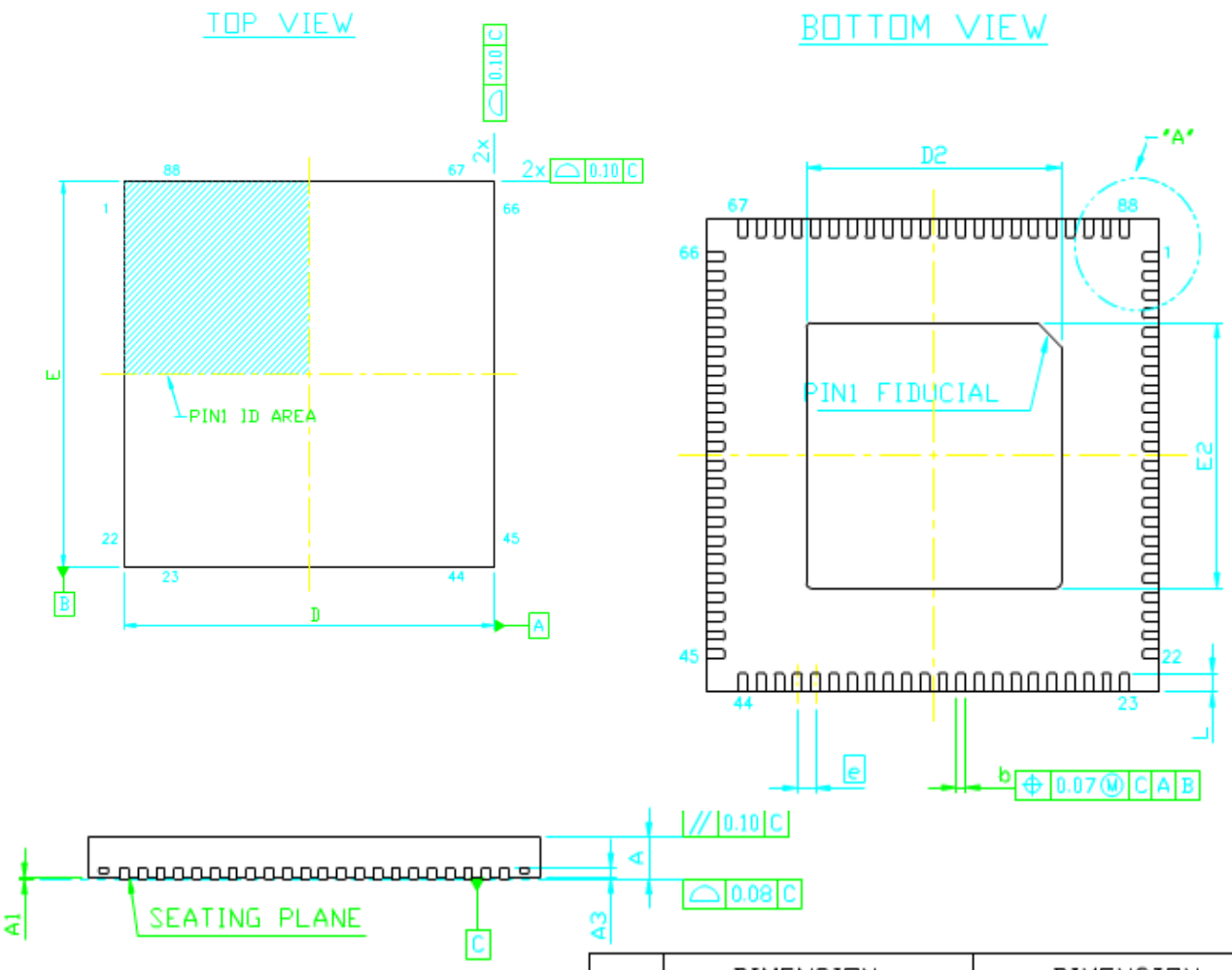
10.5.4 DSP audio quality

Test Conditions: AVDD = 2.8V, DVDD (V_{DD})= 1.8V DGND =0V, Fs= 16kHz, PGA Gain= 0dB, TA=+25°C, output loading=10K ohms, mic-in coupling capacitor= 220nF, w/ 8kHz Filter

Item	Min.	Typ.	Max.	Unit
ADC Performance				
Resolution	-	16	-	bit
Sample rate	-	16K	-	Hz
THD + N (@1kHz)	-	-60	-	dBFS
SNR (@1kHz)	85	90	-	dBFS
Dynamic range (@1kHz)	85	90	-	dBFS
Frequency response (-3dB/-9dB)	60	-	6.8K	Hz
Passband ripple	-	±0.25	-	dBFS
Single-ended full-scale input voltage	-	1.41[1]	-	Vp-p
differential full-scale input voltage	-	2.82[1]	-	Vp-p
Power supply rejection ratio (217Hz)		85		dB
Microphone/Aux Input				
Mic-in PGA gain range	0	+20 (default)	+31	dB
Aux-in PGA gain range	-12	+8 (default)	+19	dB
ADC PGA gain step	-	1	-	dB/Step
Mic input impedance	-	15K	-	Ω
Aux input impedance		60K		Ω
Microphone bias voltage	-	1.9	-	V
DAC Performance (10K Ohm Line Loading)				
Resolution	-	16	-	Bits
Sample rate		16K		Hz
THD + N (@1kHz)	-	-67.5	-	dBFS
SNR (@1kHz)	-	90	-	dBFS
Dynamic range (@1kHz)	-	85.5	-	dBFS
Frequency response (-3dB/-3dB)	20	-	6.8K	Hz
Passband ripple	-	+-0.1	-	dBFS
Single-ended full-scale output voltage	-	1.41	-	Vp-p
Differential full-scale output voltage	-	2.82	-	Vp-p
Power supply rejection ratio (217Hz)		80		dB
DAC/Analog Output Gain				
DAC PGA gain range	-31	-17 (default)	0	dB
DAC PGA gain step	-	1	-	dB/Step

Note: Although the full-scale input voltage can be as high as 1.55Vp-p, the recommended max input voltage is below 1.41Vp-p (500mVrms) for single-ended input and 2.82Vp-p (1.0Vrms) for differential input to reserve the best signal linearity.

11 Package dimensions



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	31.5	33.5	35.4
A1	0.00	0.02	0.05	0	0.8	2
A3		0.203 REF			8 REF	
b	0.15	0.20	0.25	5.9	7.8	9.8
D	9.90	10.00	10.10	389.7	393.7	397.6
D2	5.45	5.60	5.75	214.5	220.5	226.4
E	9.90	10.00	10.10	389.7	393.7	397.6
E2	5.45	5.60	5.75	214.5	220.5	226.4
L	0.30	0.40	0.50	11.8	15.7	19.7
e		0.40 BSC			15.7 BSC	
R	0.075			2.9		