2X30W Stereo Class D Audio Amplifier with PL function

General Description

The HAA3605 is an analog input, stereo, high efficiency Class D audio power amplifier. It operates from 4.5V to 16V power supply and can driver 2x4Ω speakers and delivering 2X25W peak output power (THD+N=1%) at 16V supply voltage.

The HAA3605 features PLAGC technology which constantly monitors output power and dynamically adjust internal gain to prevent long time overstress across the speaker. It also prevents clip-noise while playing music.

The HAA3605 features SSM (spread spectrum modulation), AERC (active edge rate control) and De-phase function to suppress EMI which enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements for system cost reduction.

The HAA3605 features UVP (under-voltage protection), OVP (over-voltage protection), DC speaker protection, OCP (over-current protection), OTP (over-temperature protection). All of these protections can be recovered automatically.

The HAA3605 is available in ETSSOP-28L package.

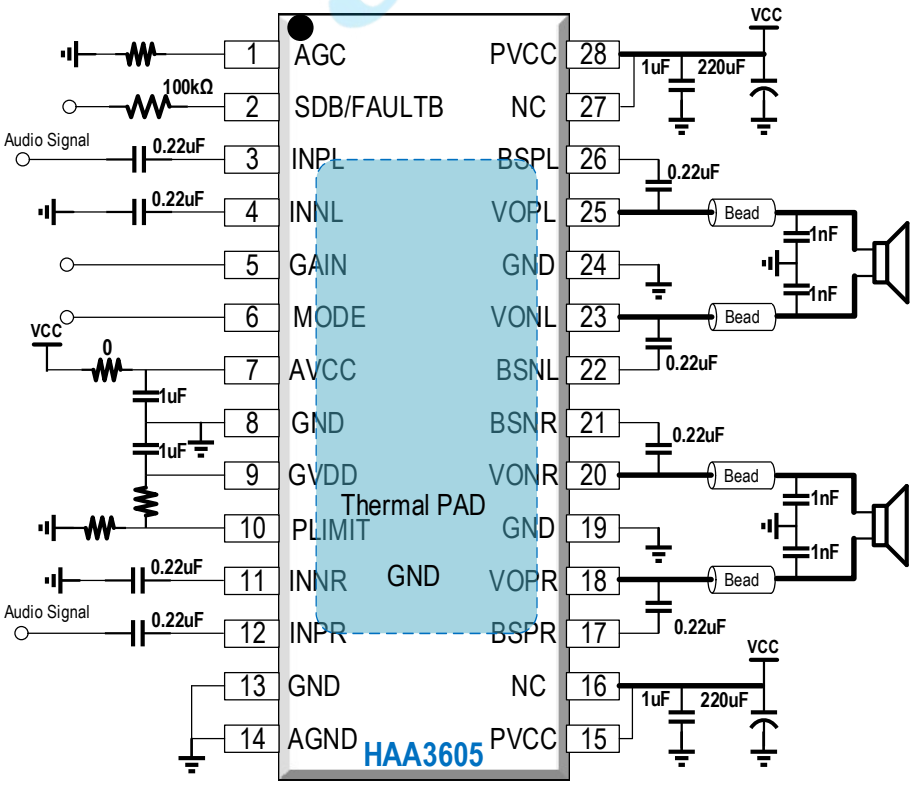
Features

- Wide Power Supply: 4.5V~16V
- 2x31.8W Output Power (4Ω @ 16V, THD+N=10%)
- 2x25.8W Output Power (4Ω @ 16V, THD+N=1%)
- 10mA Low Quiescent Supply Current
- BD, 1SPW Operation Mode Selectable
- PBTL Output Mode
- 20dB, 26dB, 32dB Gain Selectable
- Built-in Power-Limit function
- Built-in AGC function
- Built-in SSM, AERC and De-phase function
- DCP, UVP, OVP, OCP, OTP
- Built-in Pop-and-click noise suppression
- Available in ETSSOP-28L Package

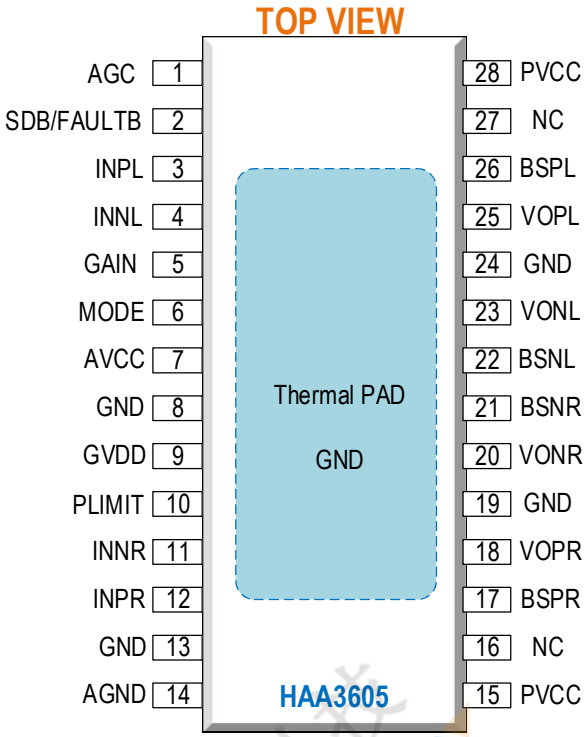
Applications

- Televisions and Monitors
- BT Speakers & Wireless Speakers
- Sound bars

Simplified Application Diagram



Pin Configuration



Pin Functions

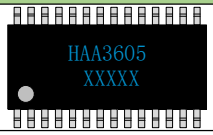
No	Name	Type	Description
1	AGC	I	AGC function Pin, connect a resistor to GND.
2	SDB/FAULTB	IO	Shutdown control pin. Low: shutdown, High: wakeup. Fault reporting when DCP, OCP, OTP.
3	INPL	I	Positive audio input for left channel. Connect to GND for PBTL mode
4	INNL	I	Negative audio input for left channel. Connect to GND for PBTL mode
5	GAIN	I	Gain control pin.
6	MODE	I	Mode control pin. Low: BD mode, High: 1SPW mode.
7	AVCC	P	Analog power supply.
8	GND	G	Ground.
9	GVDD	O	Gate driver power supply.
10	PLIMIT	I	Power-limit control. Connect a resistor divider from GVDD to GND to set power limit level.
11	INNR	I	Positive audio input for right channel.
12	INPR	I	Negative audio input for right channel
13	GND	G	Ground.
14	AGND	G	Ground.
15	PVCC	P	Power supply for right channel.
16	NC	-	No Connect Pin, connect to PVCC.
17	BSPR	O	Bootstrap supply for right channel, positive high-side power nLDMOS.
18	VOPR	O	Positive audio output for right channel.
19	GND	G	Power ground for right channel.
20	VONR	O	Negative audio output for right channel.
21	BSNR	O	Bootstrap supply for right channel, negative high-side power nLDMOS.

22	BSNL	O	Bootstrap supply for left channel, negative high-side power nLDMOS.
23	VONL	O	Negative audio output for left channel.
24	GND	G	Power ground for left channel.
25	VOPL	O	Positive audio output for left channel.
26	BSPL	O	Bootstrap supply for left channel, positive high-side power nLDMOS.
27	NC	-	No Connect Pin, connect to PVCC.
28	PVCC	P	Power supply for left channel.
Thermal PAD			Connect to GND for best thermal and electrical performance.

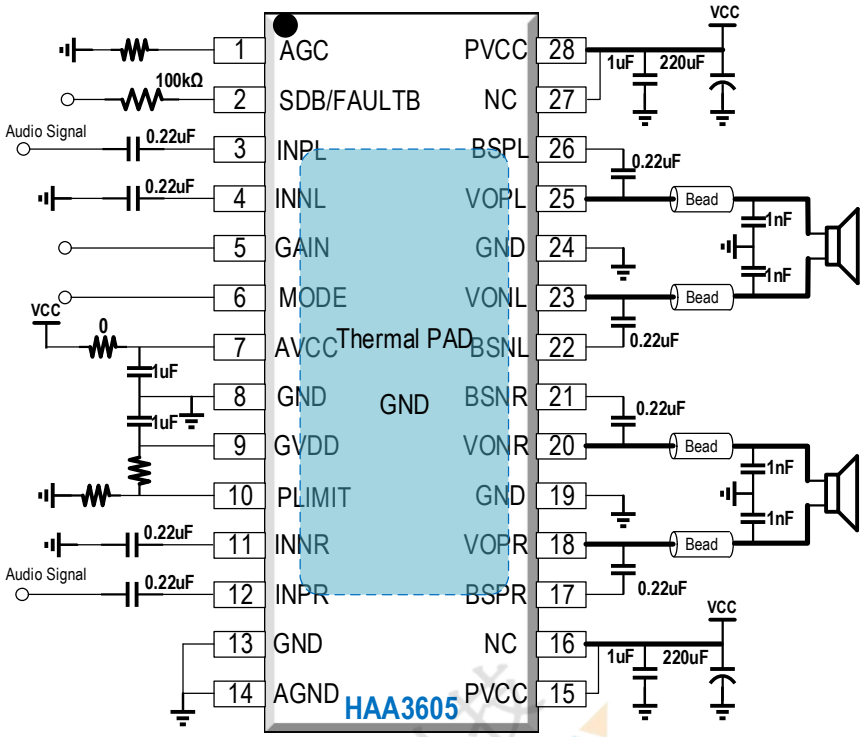
Operating Control Description

PIN Name	Connection Method		Mode Description
SDB/FAULTB	High		Startup
	Low		Shutdown
MODE	High or Floating		1SPW Mode
	Low		BD Mode
GAIN **AGC**	AGC = Floating	GAIN = GND	AGCOFF, Gain = 20dB
		GAIN = AVCC/Floating	AGCOFF, Gain = 26dB
	AGC Connect 200kΩ to GND	GAIN = GND	AGC3, Gain = 26dB
		GAIN = AVCC/Floating	AGC3, Gain = 32dB
	AGC Connect 100kΩ to GND	GAIN = GND	AGC2, Gain = 26dB
		GAIN = AVCC/Floating	AGC2, Gain = 32dB
	AGC Connect 50kΩ to GND	GAIN = GND	AGC1, Gain = 26dB
		GAIN = AVCC/Floating	AGC1, Gain = 32dB
	AGC = GND	GAIN = GND	AGCOFF, Gain = 26dB
		GAIN = AVCC/Floating	AGCOFF, Gain = 32dB
INPL, INNL	Both to GND		PBTL Mode

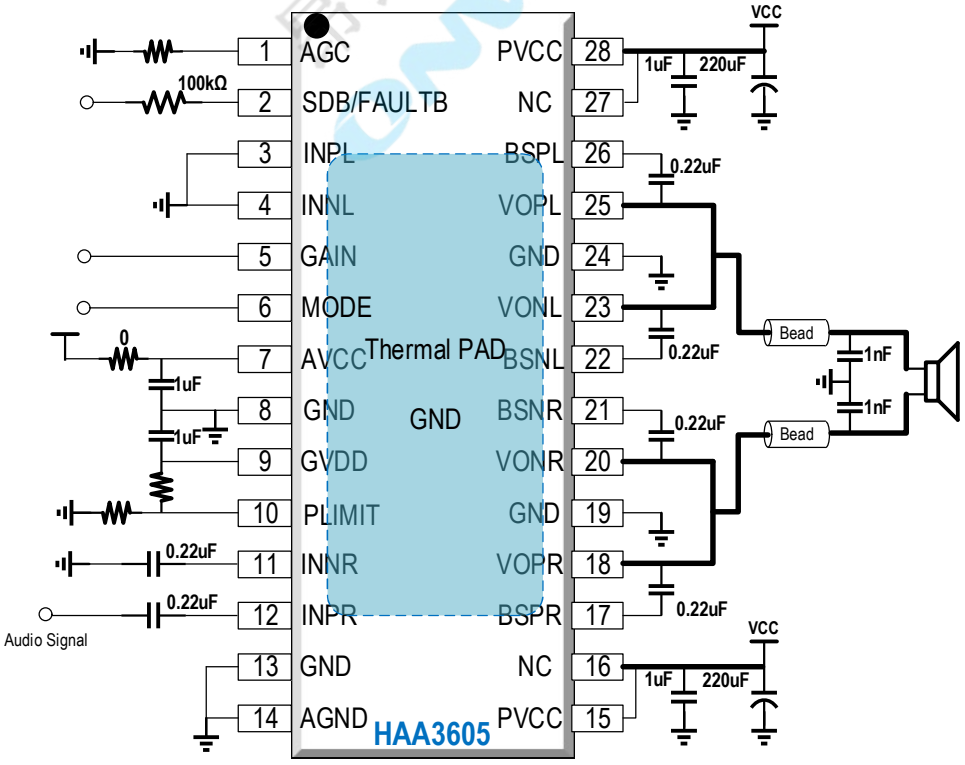
Order Information

Part No.	Package	Mark	Tape and Reel Information
HAA3605	ETSSOP-28L		2500pcs/Reel

Typical Application Circuits



BTL Configuration with Single-Ended Inputs



PBTL Configuration with Single-Ended Inputs

Absolute Maximum Ratings

Over operating free–air temperature range, TA= 25°C (unless otherwise noted)(1)

Parameter		Min	Max	Unit
Supply Voltage	AVCC, PVCC	-0.3	18	V
Input Voltage	SDB/FAULTB, GAIN, MODE	-0.3	AVCC+0.3	V
	INL, IPL, INR, IPR	-0.3	5.5	V
	PLIMIT, AGC	-0.3	GVDD+0.3	V
Operating free-air temperature range T_A		-40	85	°C
Operating junction temperature range T_J		-40	150	°C
Storage temperature range T_{STG}		-65	150	°C
ESD Ratings				
Human Body Model (HBM) ESD(2)		±2000		V
Charged Device Model (CDM) ESD(2)		±500		V
Thermal Metric				
θ_{JA} Junction-to-ambient thermal resistance		30.3		°C /W
$\theta_{JC(top)}$ Junction-to-case (top) thermal resistance		33.5		°C /W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) This device series contains ESD protection and passes the following tests:

Human Body Model (HBM) standard: ESDA/JEDEC JS-001-2017 for all pins.

Charged Device Model (CDM) standard: ANSI/ESDA/JEDEC JS-002-2018 for all pins.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Electrical Characteristics

AVCC=PVCC=12V, T_A = 25°C, R_L = 4Ω+33μH, Cin = 0.22μF, BD Mode (unless otherwise noted)

Parameter		Condition & Description				Min	Typ	Max	Unit
Vcc	Supply voltage	PVCC, AVCC				4.5		16	V
GVDD	Gate drive supply	SD/FAULT=GND, I_{GVDD}=2mA				4.8	5	5.2	V
Isd	SD current						10		μA
Iq	Quiescent current						9.6		mA
UVP	Under voltage protection	BD Mode					7.5		V
		1SPW Mode					3.4		
OVP	Over voltage protection						17.5		V
OTP	Over temperature protection						155		℃
Ton	Turn on time						50		ms
Toff	Turn off time						12.6		us
Input PIN(1)									
V_{IH}	High logic input	SDB/FAULTB, GAIN,				2		AVCC	V
V_{IL}	Low logic input					0		0.65	V
V_{OL}	Low logic output	SDB/FAULTB, 100kΩ pull-up resistor						0.6	V
Class D									
V_{OS}	Output offset Voltage	Gain=26dB, CPK=2				-10	0	10	mV
	Quiescent Output Duty-Cycle	BD Mode					50		%
		1SPW Mode					16		
f_{CLK}	OSC frequency						330		kHz
	SSM frequency Range					-10.5		10.5	%
Po(2)	Output power	BD BTL	2 x 8Ω	8V	THD+N=1%		3.75		W
					THD+N=10%		4.62		
				12V	THD+N=1%		8.3		
					THD+N=10%		10.3		
				16V	THD+N=1%		14.8		
					THD+N=10%		18.3		
			2 x 6Ω	8V	THD+N=1%		4.89		
					THD+N=10%		6.05		
				12V	THD+N=1%		10.98		
					THD+N=10%		13.56		
				16V	THD+N=1%		19.3		
					THD+N=10%		23.8		
			2 x 4Ω	8V	THD+N=1%		6.9		
					THD+N=10%		8.5		
				12V	THD+N=1%		15.2		
					THD+N=10%		18.5		
				16V	THD+N=1%		25.8		
					THD+N=10%		31.8		
		BD PBTL	4Ω	8V	THD+N=1%		7.55		
					THD+N=10%		9.3		

				12V	THD+N=1%		16.8		
					THD+N=10%		20.8		
				16V	THD+N=1%		29.6		
					THD+N=10%		36.6		
			2Ω	8V	THD+N=1%		13.5		
					THD+N=10%		16.6		
				12V	THD+N=1%		29.6		
					THD+N=10%		36.6		
				16V	THD+N=1%		52.8		
					THD+N=10%		63.8		
Po[2]	Output power	1SPW BTL	2 x 8Ω	8V	THD+N=1%		3.76		W
					THD+N=10%		4.63		
				12V	THD+N=1%		8.42		
					THD+N=10%		10.41		
				16V	THD+N=1%		14.9		
					THD+N=10%		18.35		
			2 x 6Ω	8V	THD+N=1%		4.87		
					THD+N=10%		6.05		
				12V	THD+N=1%		10.96		
					THD+N=10%		13.6		
				16V	THD+N=1%		19.2		
					THD+N=10%		23.6		
			2 x 4Ω	8V	THD+N=1%		6.92		
					THD+N=10%		8.5		
				12V	THD+N=1%		15.36		
					THD+N=10%		18.65		
				16V	THD+N=1%		26.3		
					THD+N=10%		32.2		
		1SPW PBTL	4Ω	8V	THD+N=1%		7.545		
					THD+N=10%		9.378		
				12V	THD+N=1%		16.88		
					THD+N=10%		20.8		
				16V	THD+N=1%		29.87		
					THD+N=10%		36.76		
			2Ω	8V	THD+N=1%		13.65		
					THD+N=10%		16.72		
				12V	THD+N=1%		30.05		
					THD+N=10%		36.36		
				16V	THD+N=1%		52.3		
					THD+N=10%		64		
η	Efficiency	BTL BD	2 x 8Ω	12V	Po = 10W		92.5		%
			2 x 6Ω		Po = 11W		91.5		
			2 x 4Ω		Po = 15W		88		
		PBTL	4Ω		Po = 20W		93.1		

		BD	2Ω		Po = 30W		88.5		
		BTL 1SPW	2 x 8Ω		Po = 10W		93.3		
			2 x 6Ω		Po = 11W		92.6		
			2 x 4Ω		Po = 15W		89.6		
		PBTL 1SPW	4Ω		Po = 20W		94.1		
			2Ω		Po = 30W		90.1		
Ron	On resistance of Power MOS	0.5A, High Side					150		mΩ
		0.5A, Low Side					150		
t_{dcdet}	DC detect time						800		ms
Vn	noise	A-weighting, Gain=20dB					75		μVrms
		A-weighting, Gain=26dB					95		
		A-weighting, Gain=32dB					141		
	Crosstalk	Vo=1Vrms, Gain=26dB, f=1kHz					-101		dB
SNR	Signal-to-noise ratio	Output power at THD+N=1%					106		dB
PSRR		200mVpp ripple at 1kHz， Gain=26dB					-70		dB
THD+N	Total harmonic distortion + noise	f=1kHz,Po=5W					0.04		%
		f=1kHz,Po=12W					0.05		%
Gain(3)	Audio Gain	GAIN = GND, AGC = Floating				19	20	21	dB
		GAIN = AVCC/Floating, AGC = Floating				25	26	27	
		GAIN = GND, AGC = Other states(3)				25	26	27	
		GAIN = AVCC/Floating, AGC = Other states(3)				31	32	33	
Power Limit AGC Function									
	Max Attenuation						-12		dB
	Gain Attenuation Step						0.5		dB
Atk1	AGC1 Attack time	AGC PIN connect 50kohm to GND					60		ms
Rel1	AGC1 Release time						600		
Atk2	AGC2 Attack time	AGC PIN connect 100kohm to GND					33		
Rel2	AGC2 Release time						600		
Atk3	AGC3 Attack time	AGC PIN connect 200kohm to GND					13		
Rel3	AGC3 Release time						1200		
AGCOFF		AGC PIN Floating and connect to GND							

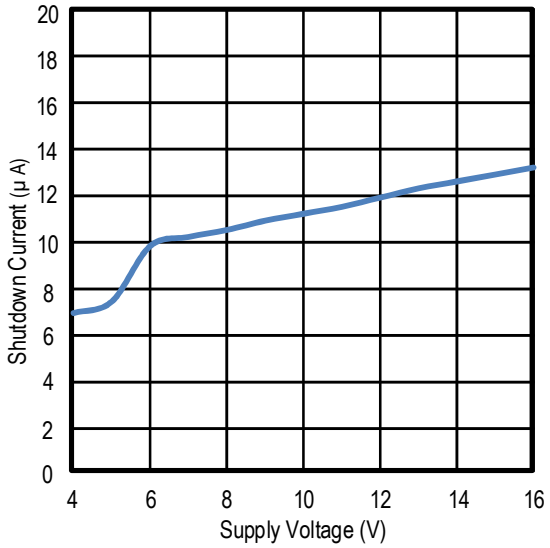
(1): Set SDB/FAULTB to high level, make sure the pull-up resistor is larger than 4.7kΩ and smaller than 500kΩ.

(2): High output power of HAA3605 needs good thermal dissipation. It will be thermal protection if the heat dissipation is not good enough. If necessary, a heat sink can be used for thermal dissipation.

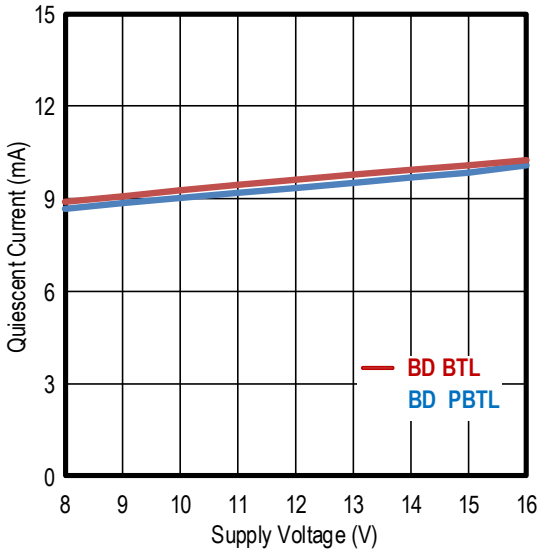
(3): See the *Operating Control Description* for other states.

Typical Characteristics

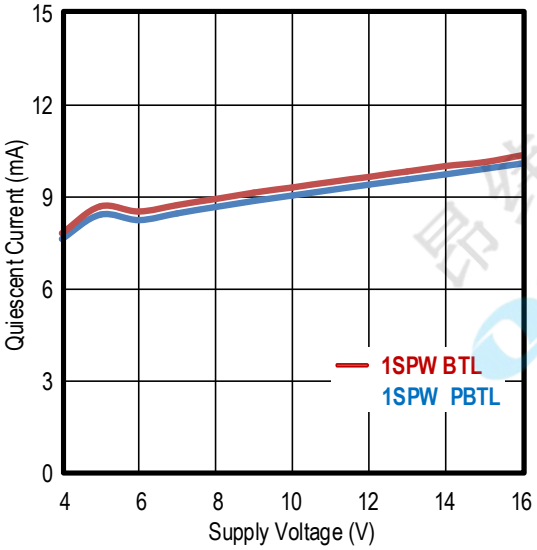
Shutdown Current vs Supply Voltage



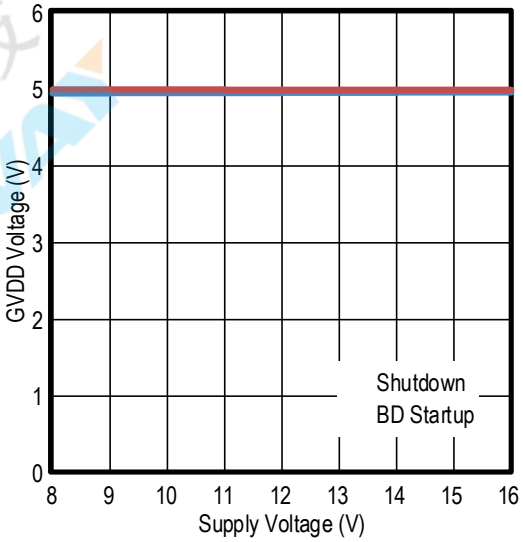
Quiescent Current vs Supply Voltage



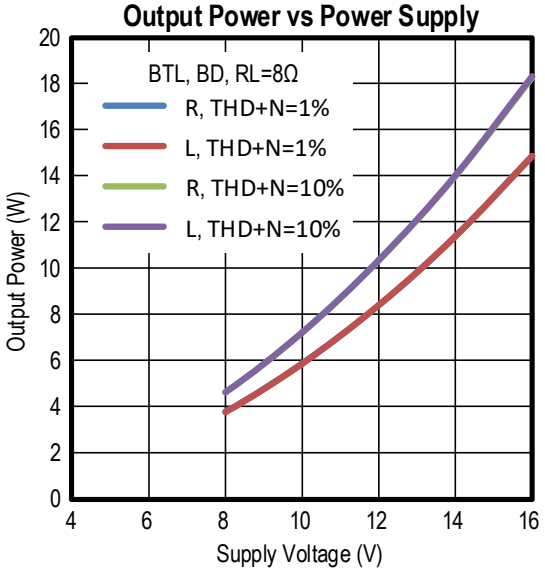
Quiescent Current vs Supply Voltage



GVDD Voltage vs Supply Voltage



Output Power vs Power Supply



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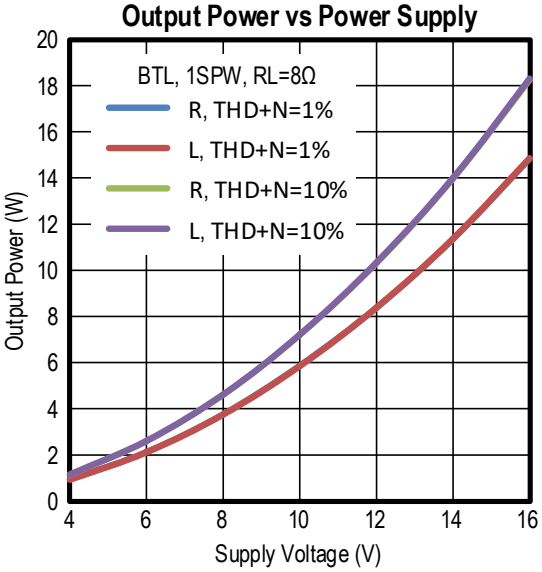

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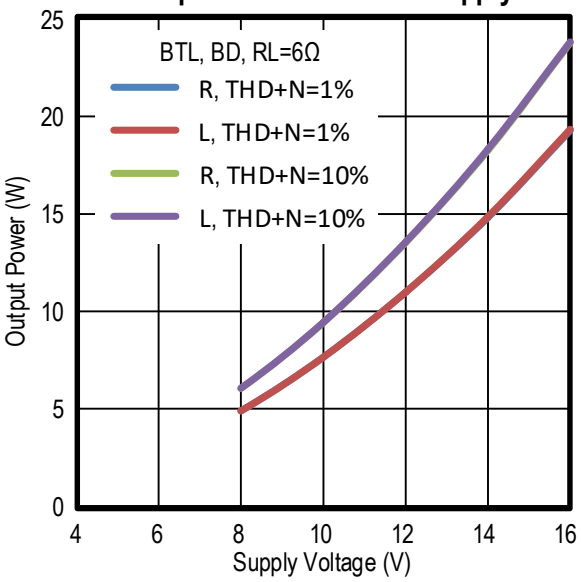

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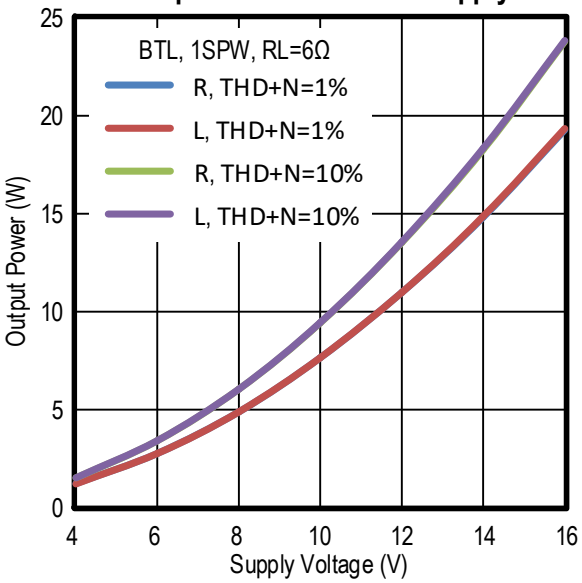
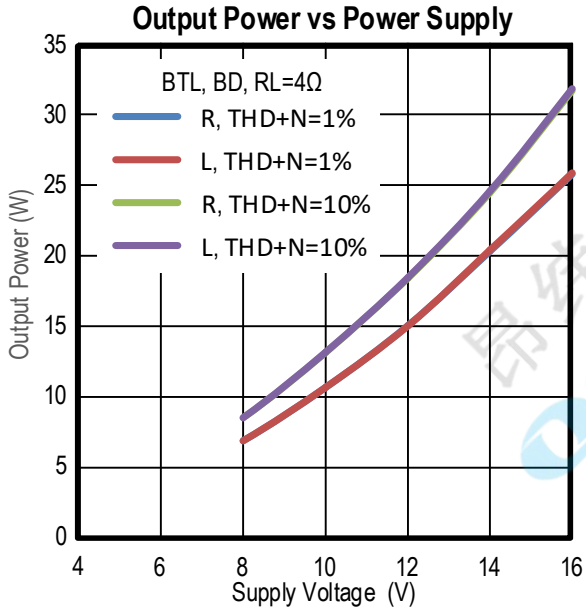
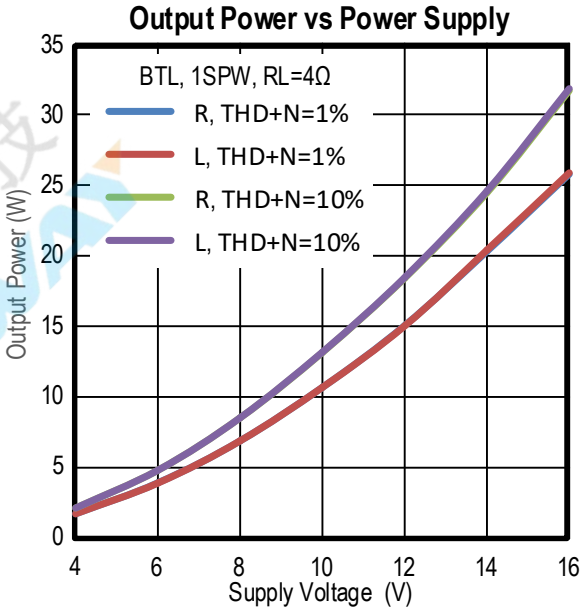


Output Power vs Power Supply



Output Power vs Power Supply



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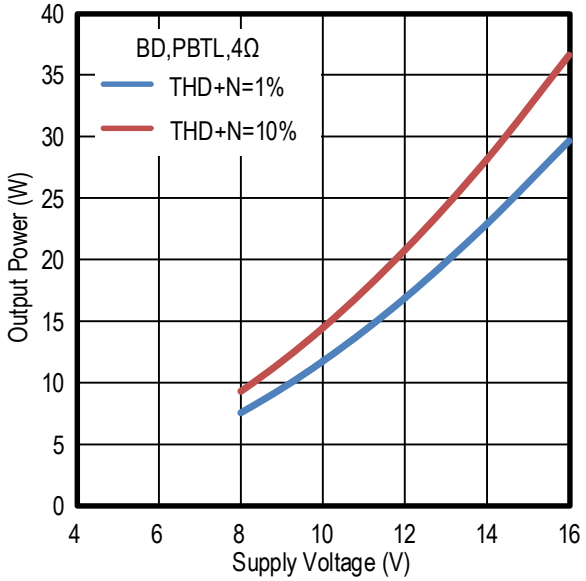
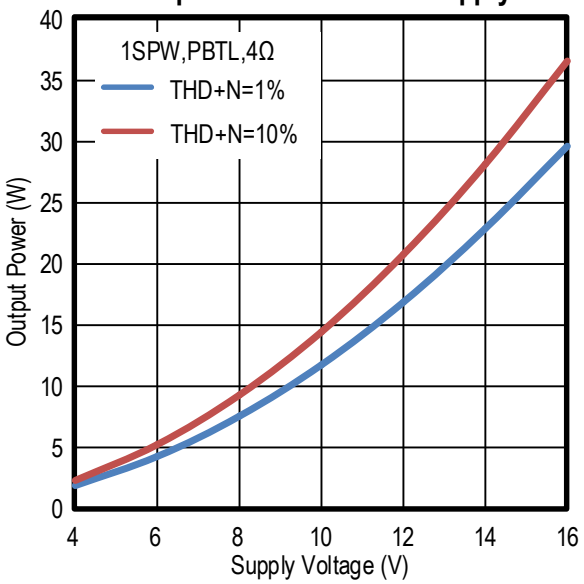


Output Power vs Power Supply



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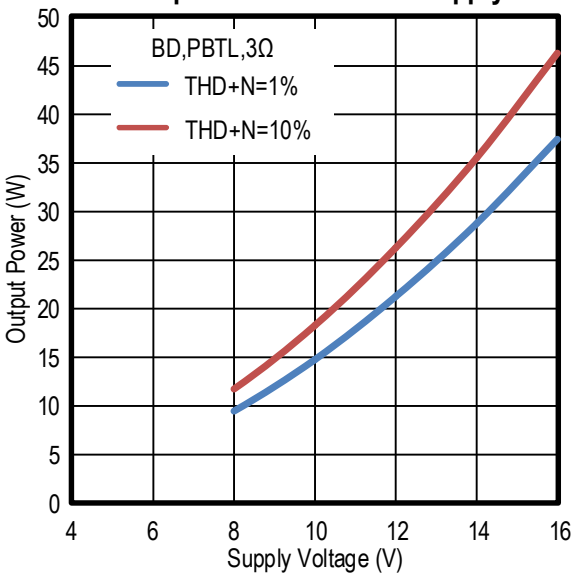

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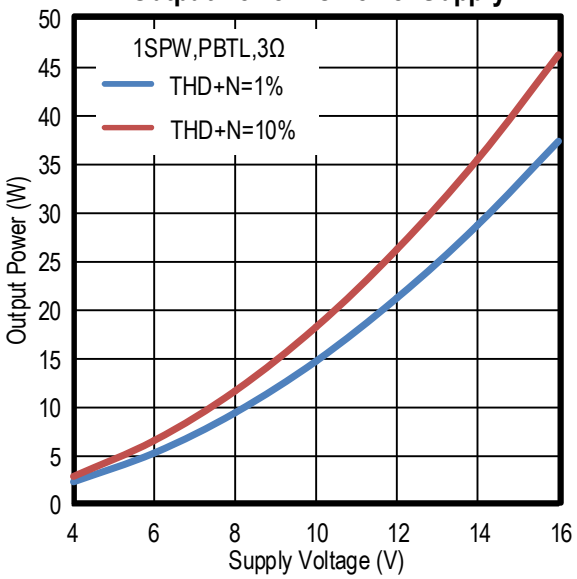

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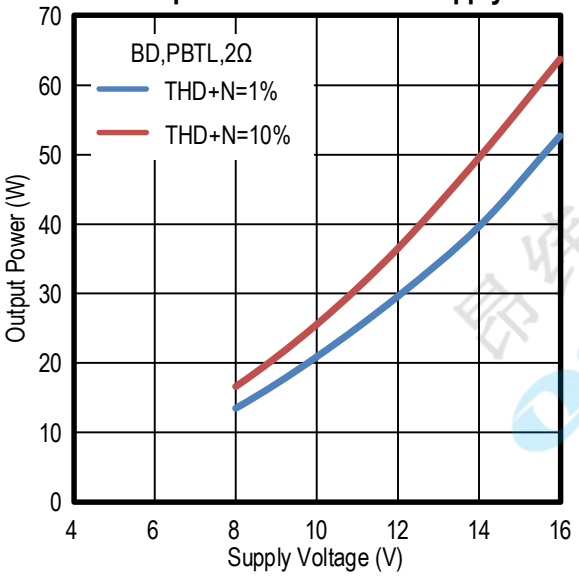
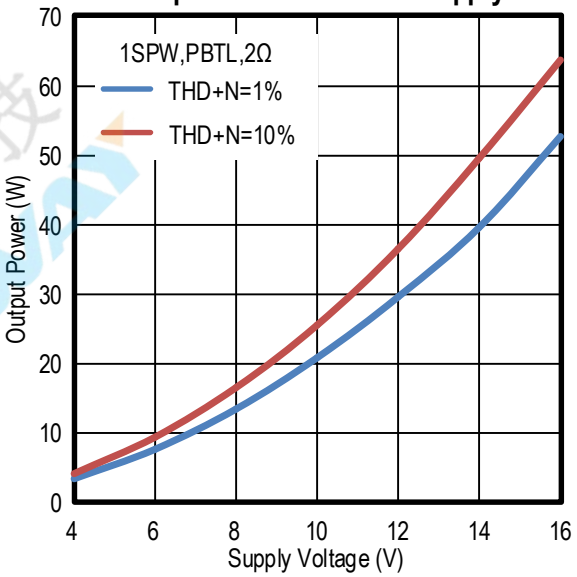
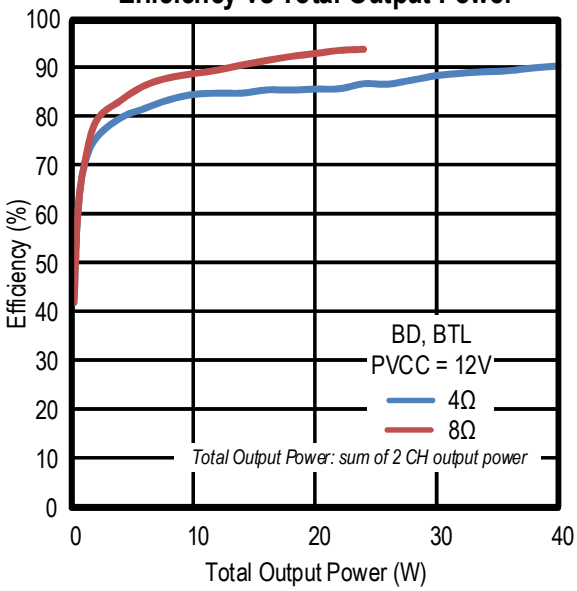


Output Power vs Power Supply



Efficiency vs Total Output Power



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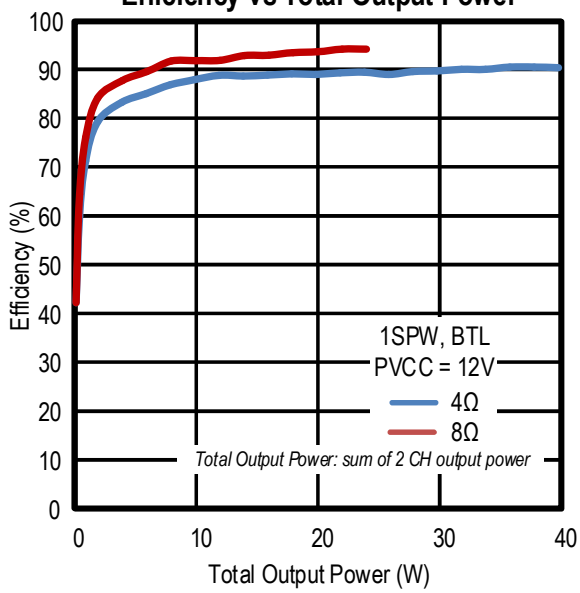
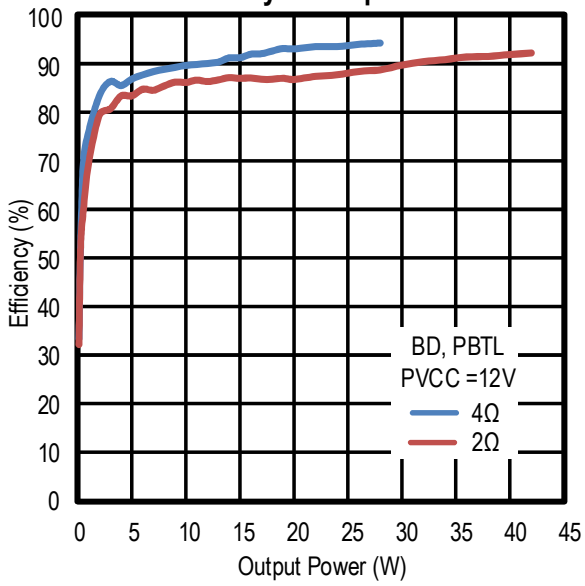
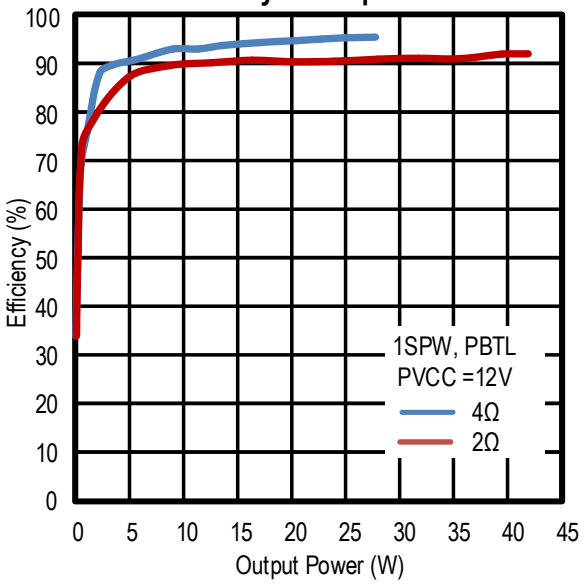


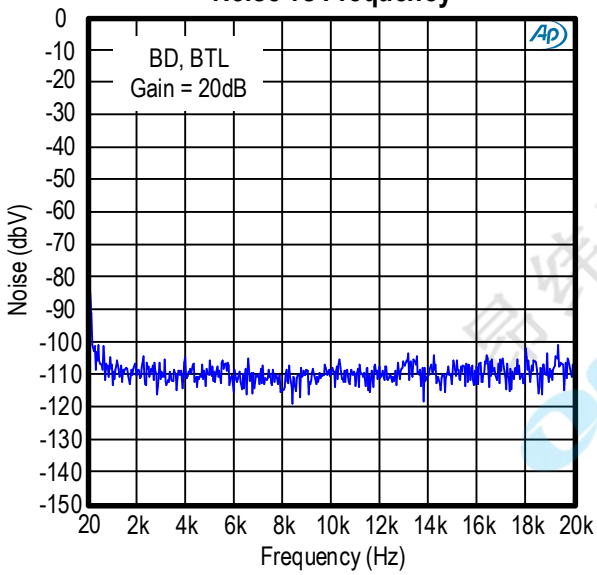
Efficiency vs Output Power



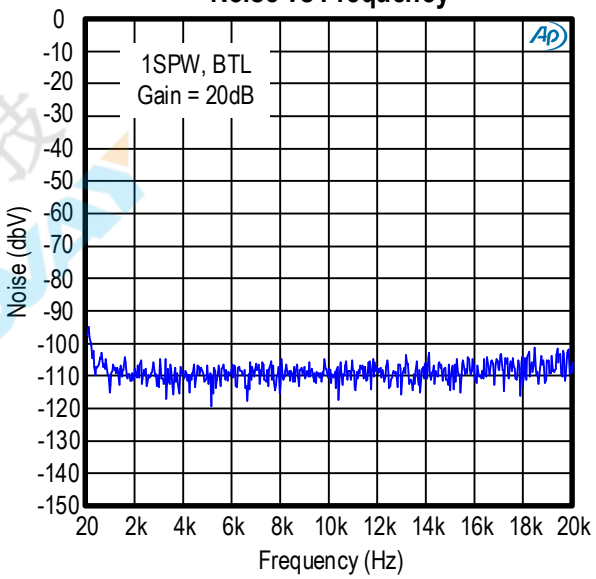
Efficiency vs Output Power



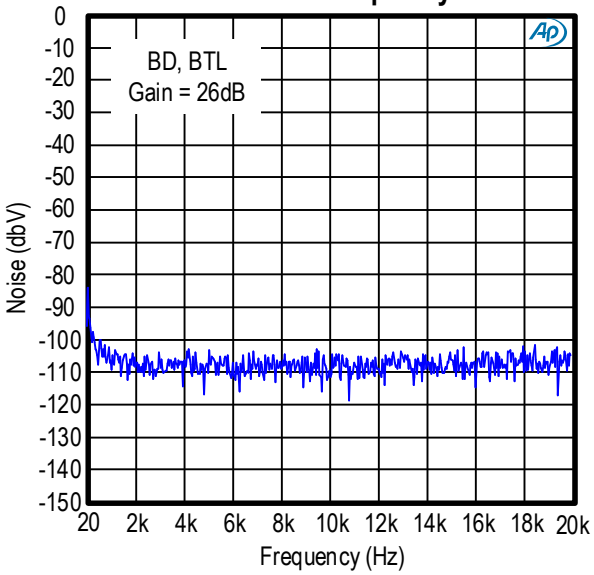
Noise vs Frequency



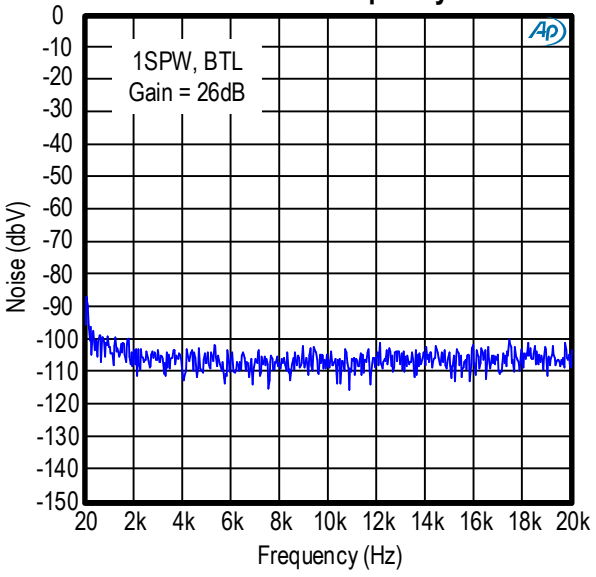
Noise vs Frequency

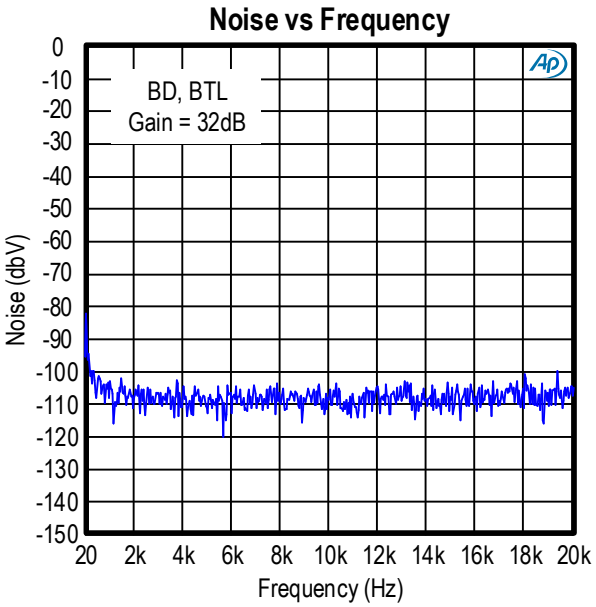


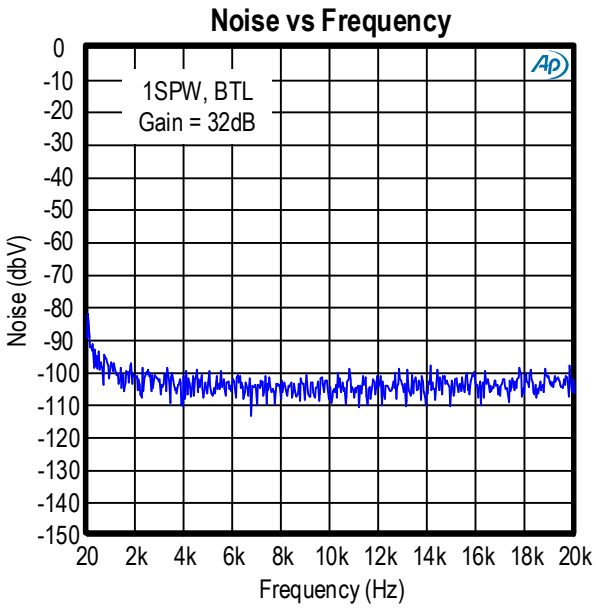
Noise vs Frequency

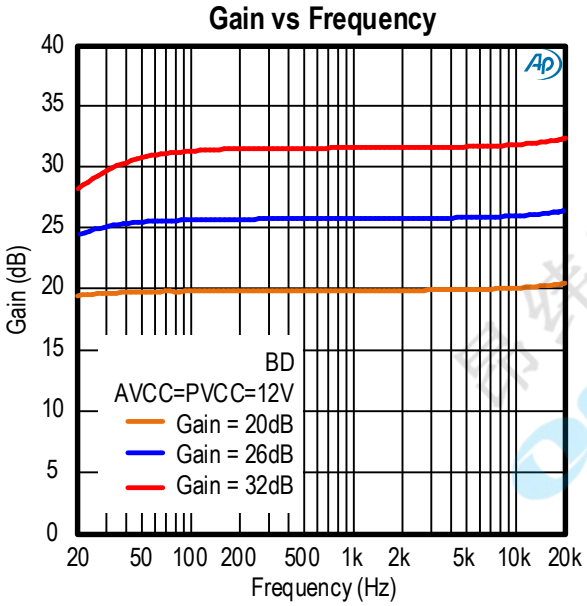


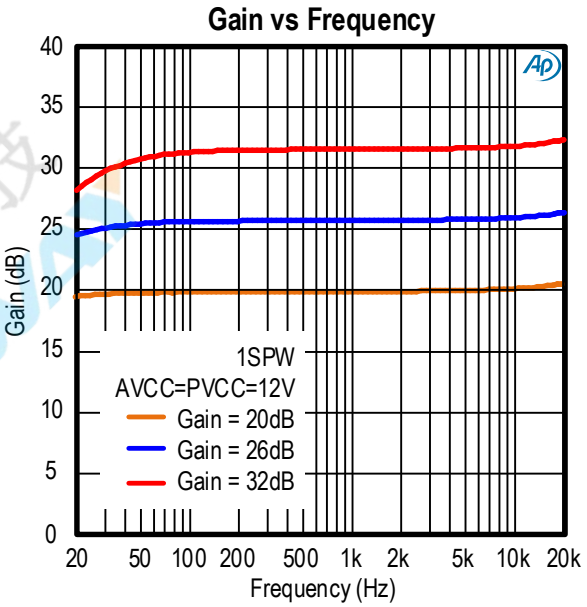
Noise vs Frequency

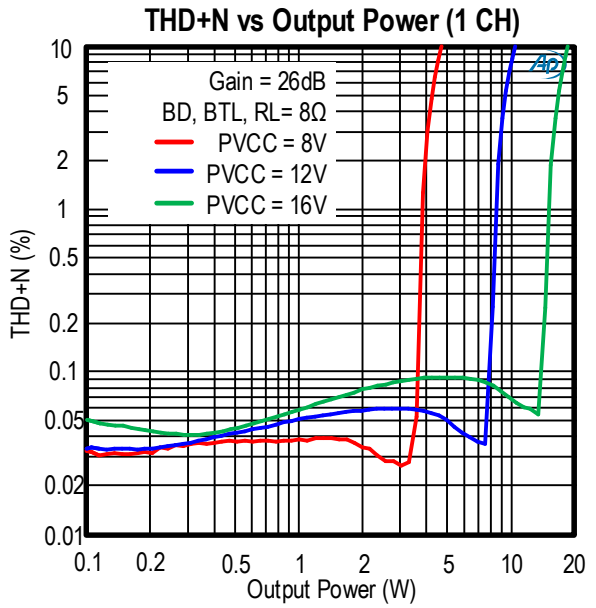


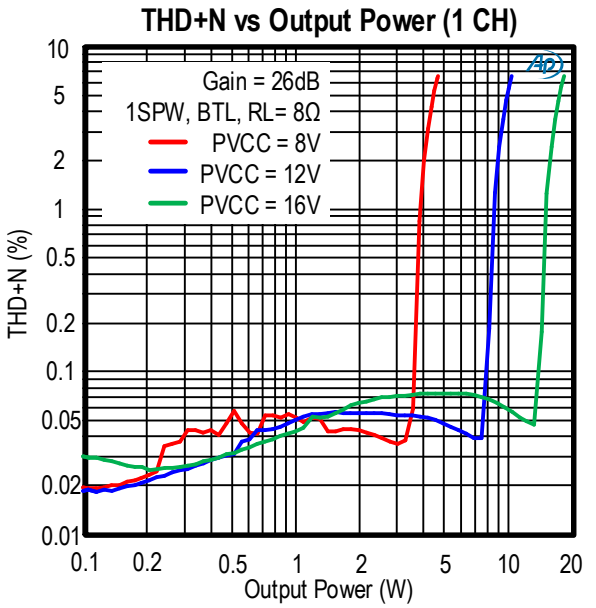

Noise vs Frequency
BD, BTL
Gain = 32dB
Noise (dbV)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
20 2k 4k 6k 8k 10k 12k 14k 16k 18k 20k
Frequency (Hz)


Noise vs Frequency
1SPW, BTL
Gain = 32dB
Noise (dbV)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
20 2k 4k 6k 8k 10k 12k 14k 16k 18k 20k
Frequency (Hz)

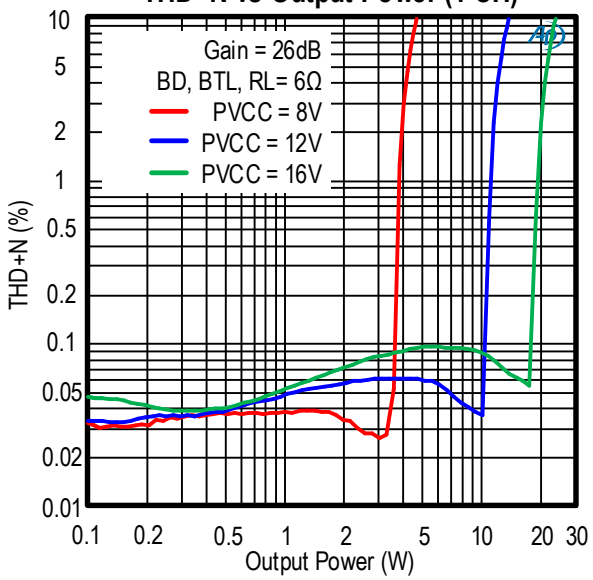

Gain vs Frequency
BD
AVCC=PVCC=12V
Gain = 20dB
Gain = 26dB
Gain = 32dB
Gain (dB)
40
35
30
25
20
15
10
5
0
20 50 100 200 500 1k 2k 5k 10k 20k
Frequency (Hz)


Gain vs Frequency
1SPW
AVCC=PVCC=12V
Gain = 20dB
Gain = 26dB
Gain = 32dB
Gain (dB)
40
35
30
25
20
15
10
5
0
20 50 100 200 500 1k 2k 5k 10k 20k
Frequency (Hz)

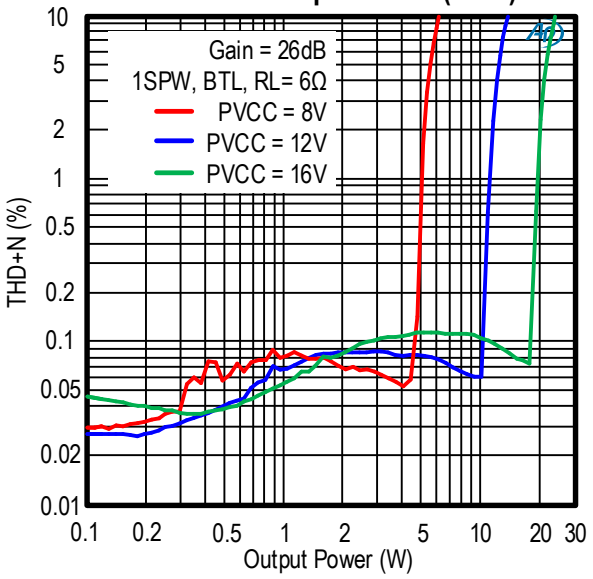

THD+N vs Output Power (1 CH)
Gain = 26dB
BD, BTL, RL= 8Ω
PVCC = 8V
PVCC = 12V
PVCC = 16V
THD+N (%)
10
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1 0.2 0.5 1 2 5 10 20
Output Power (W)


THD+N vs Output Power (1 CH)
Gain = 26dB
1SPW, BTL, RL= 8Ω
PVCC = 8V
PVCC = 12V
PVCC = 16V
THD+N (%)
10
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1 0.2 0.5 1 2 5 10 20
Output Power (W)

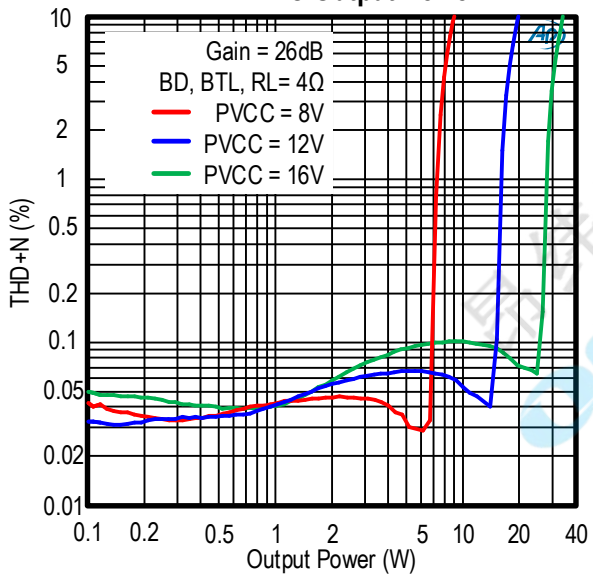
THD+N vs Output Power (1 CH)



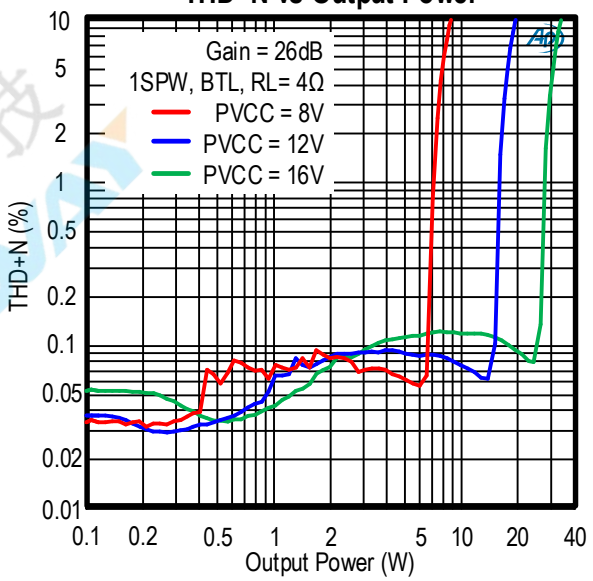
THD+N vs Output Power (1 CH)



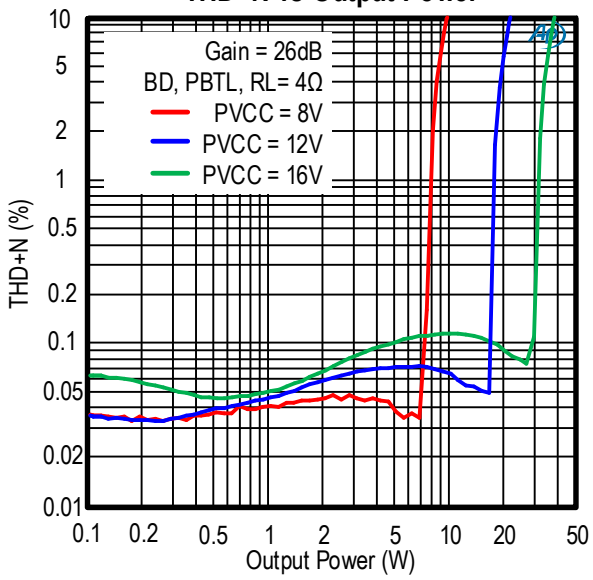
THD+N vs Output Power



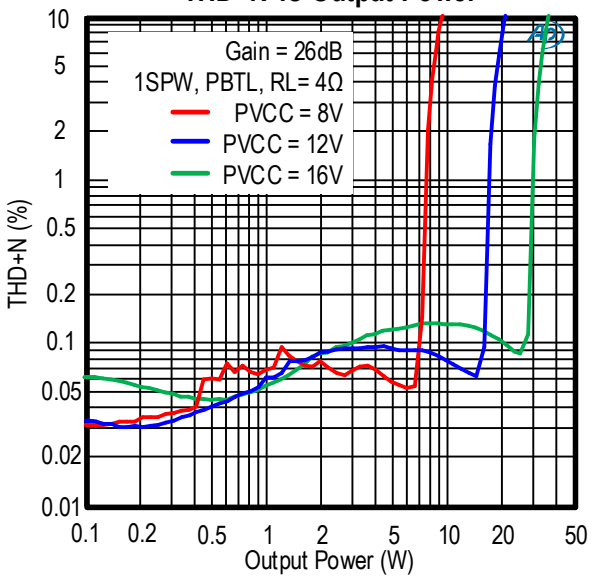
THD+N vs Output Power



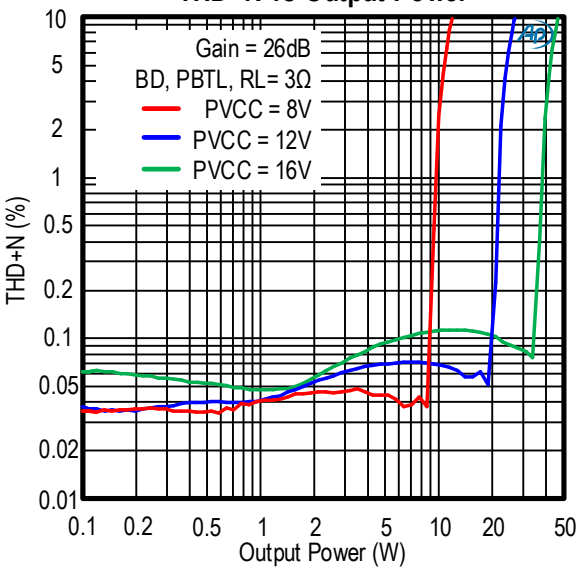
THD+N vs Output Power



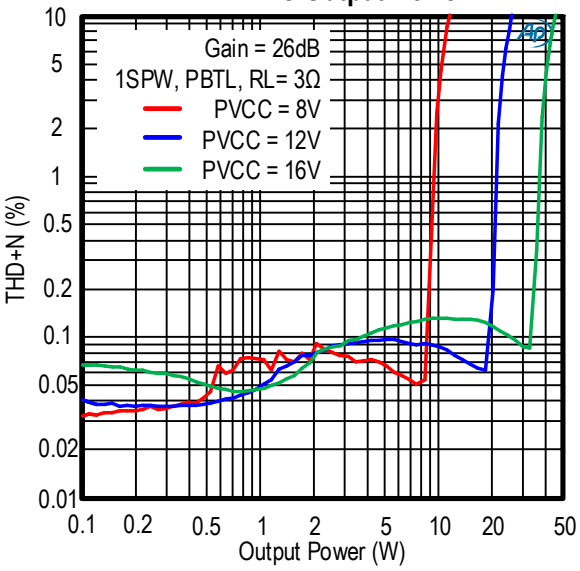
THD+N vs Output Power



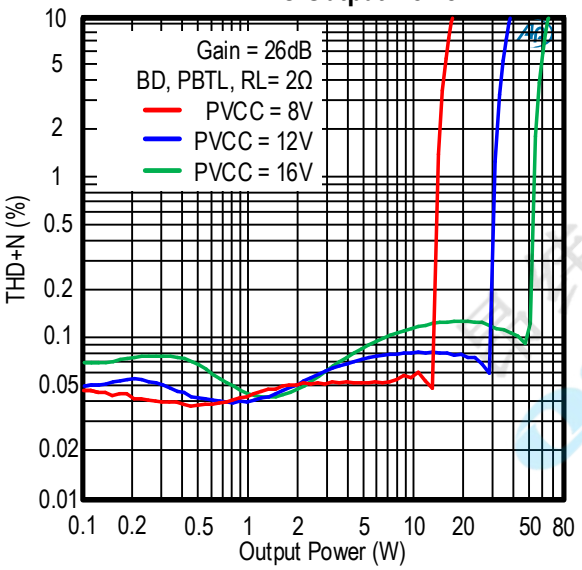
THD+N vs Output Power



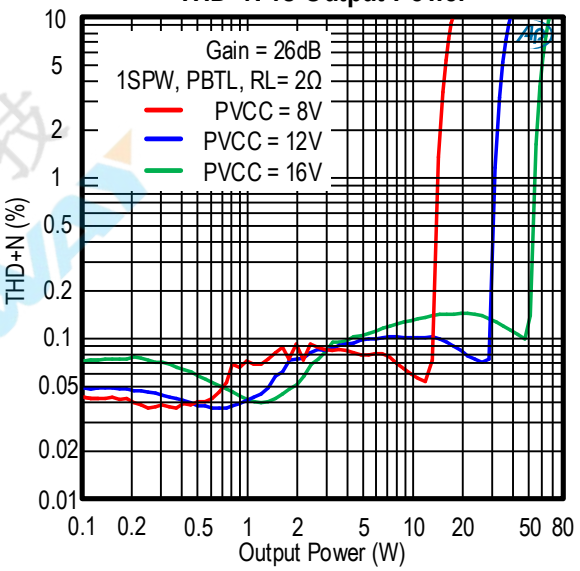
THD+N vs Output Power



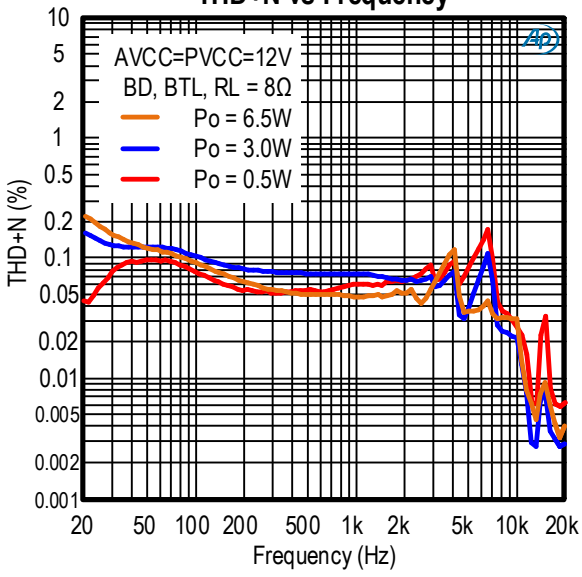
THD+N vs Output Power



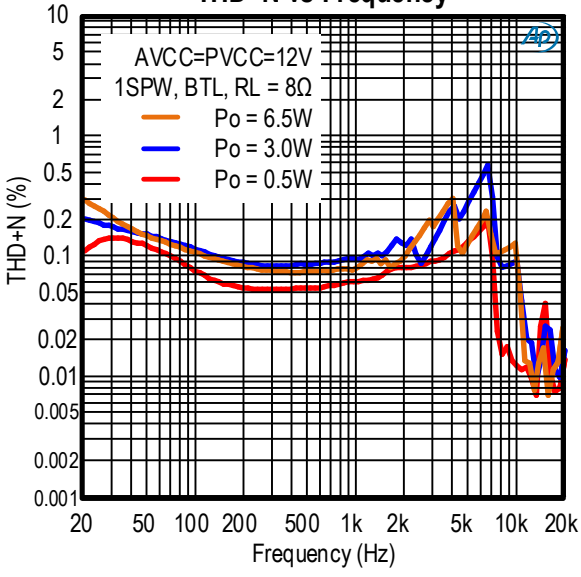
THD+N vs Output Power



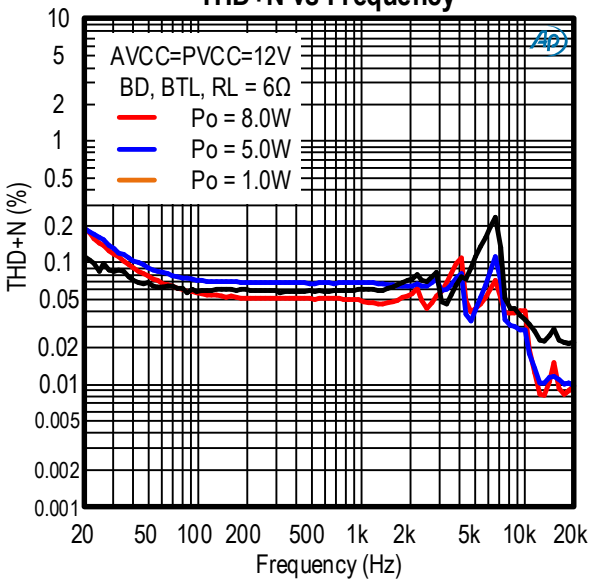
THD+N vs Frequency



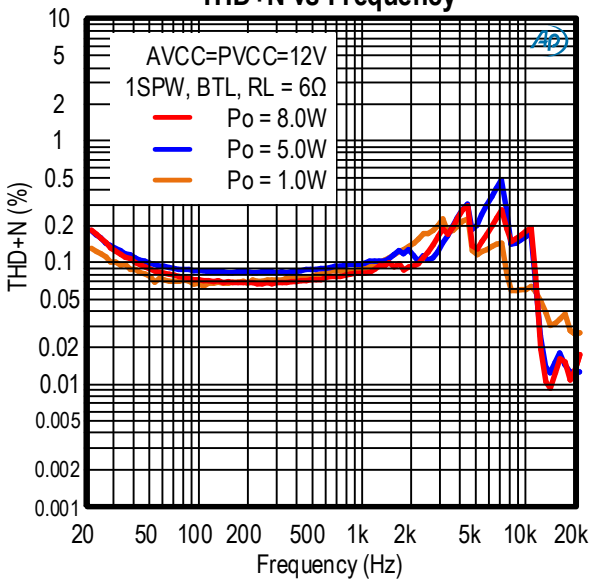
THD+N vs Frequency



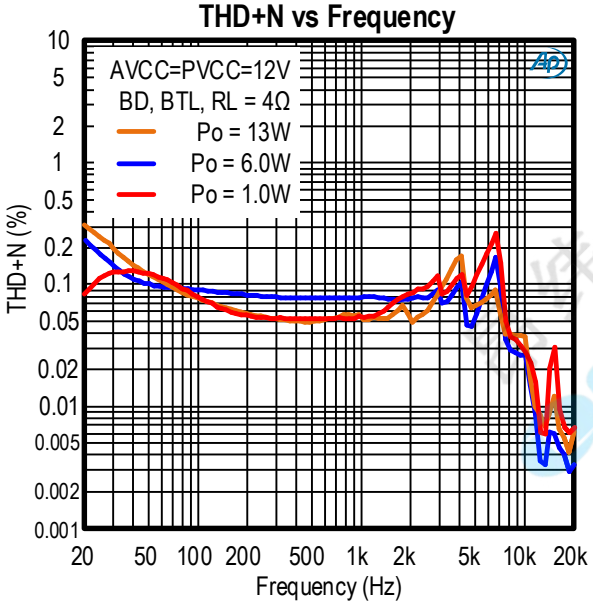
THD+N vs Frequency



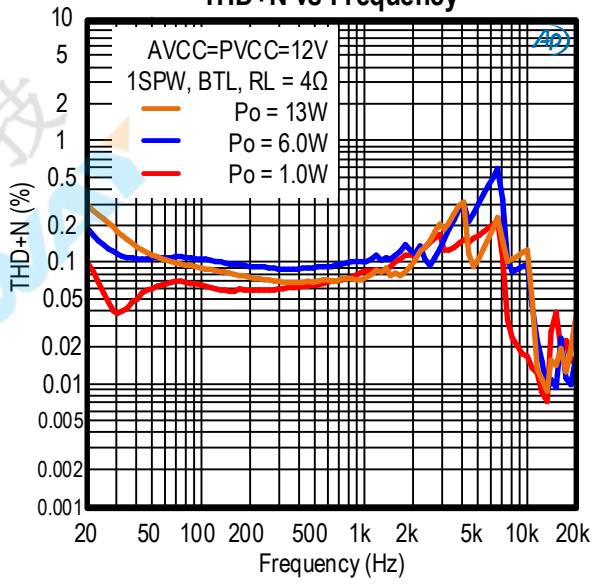
THD+N vs Frequency



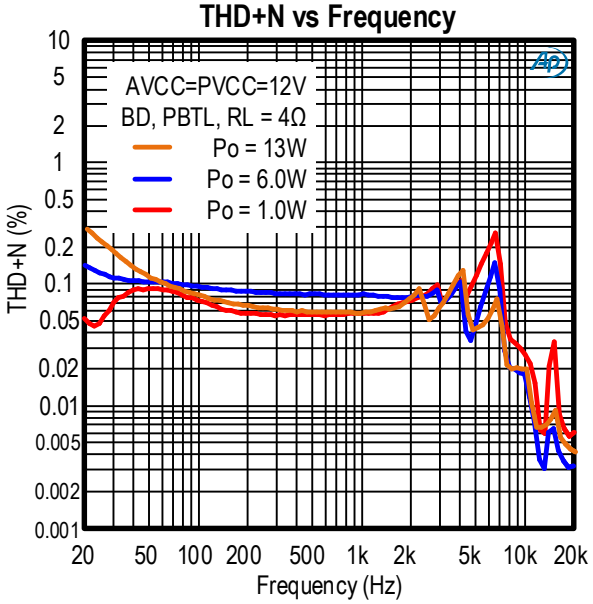
THD+N vs Frequency



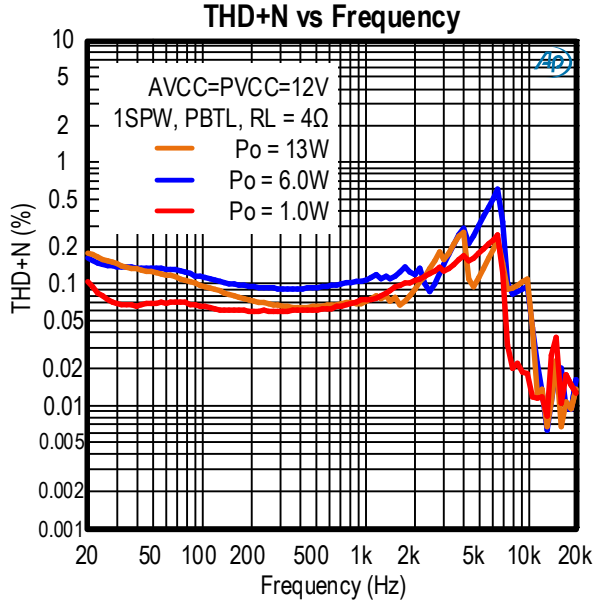
THD+N vs Frequency



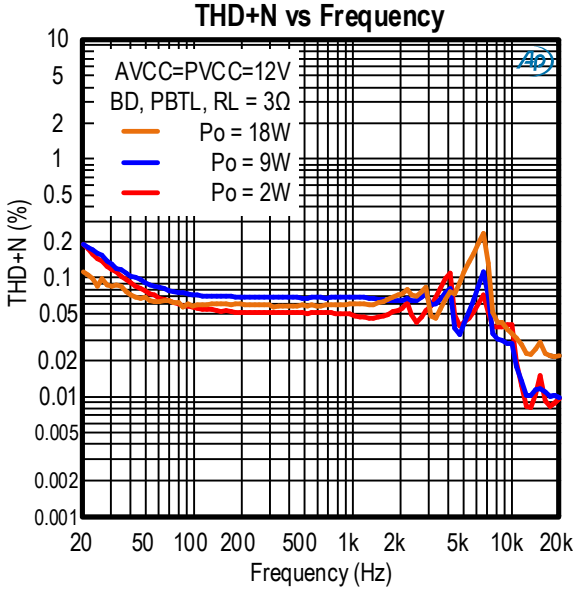
THD+N vs Frequency



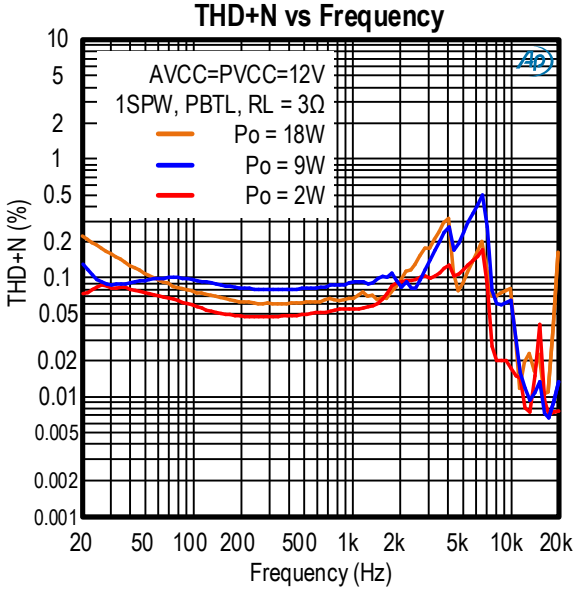
THD+N vs Frequency



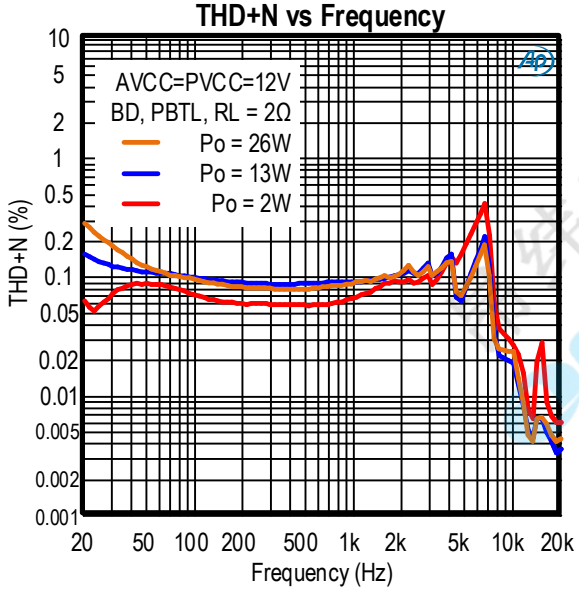
THD+N vs Frequency



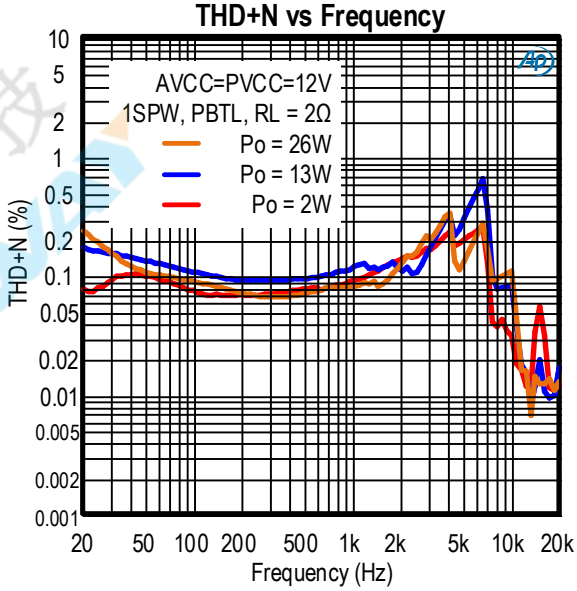
THD+N vs Frequency



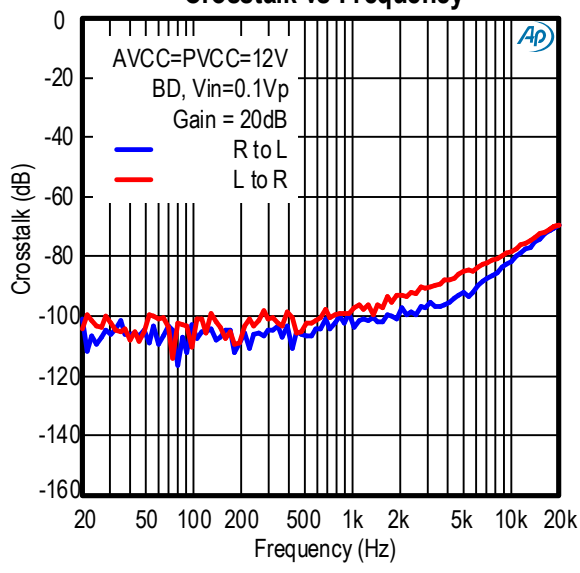
THD+N vs Frequency



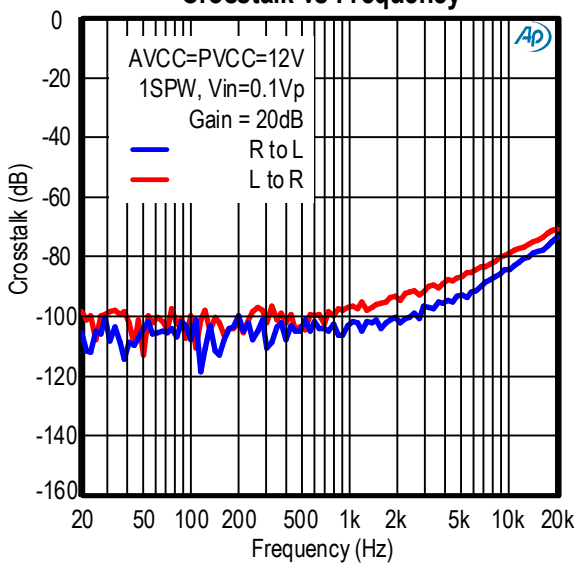
THD+N vs Frequency



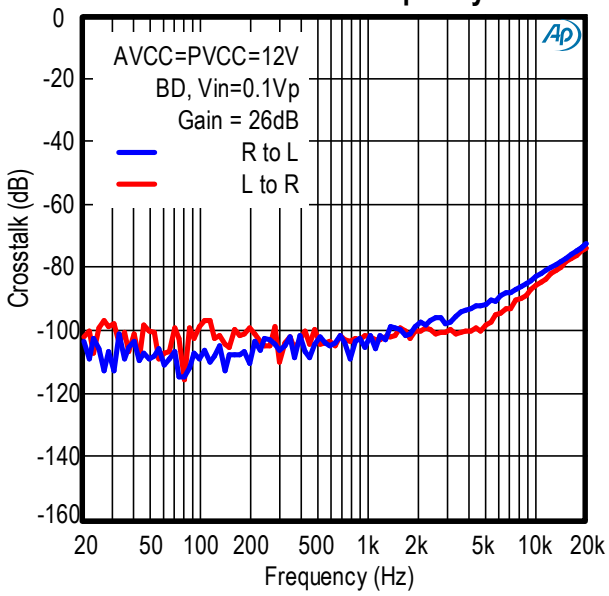
Crosstalk vs Frequency



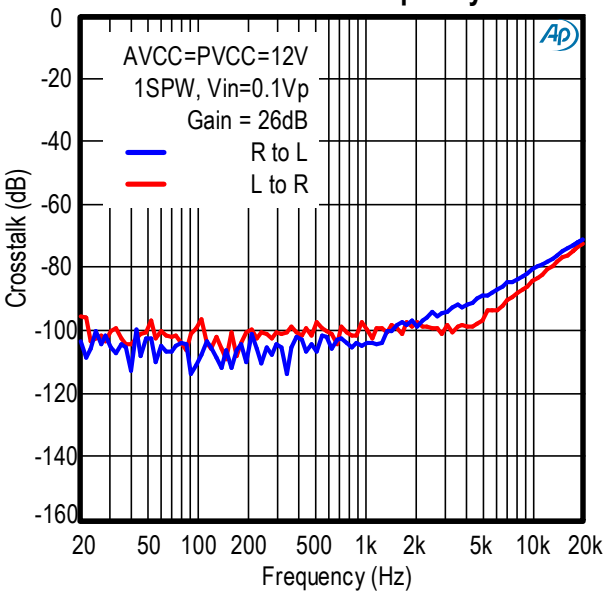
Crosstalk vs Frequency



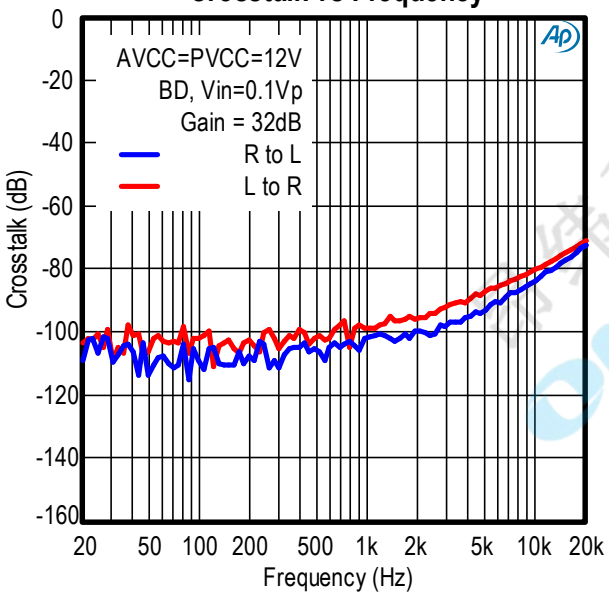
Crosstalk vs Frequency



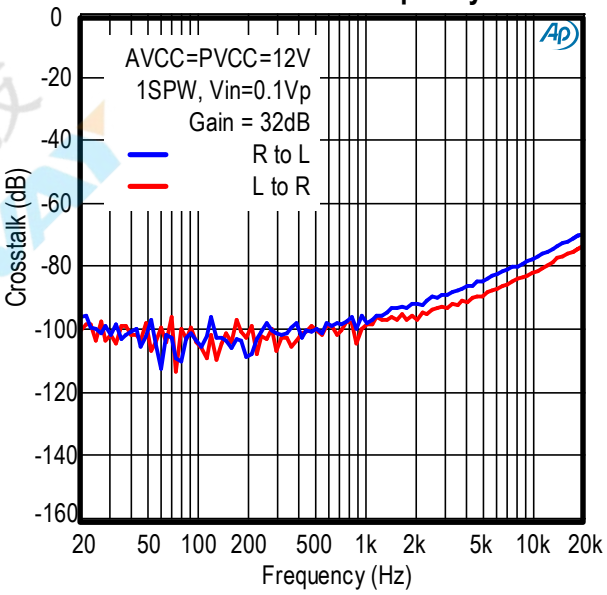
Crosstalk vs Frequency



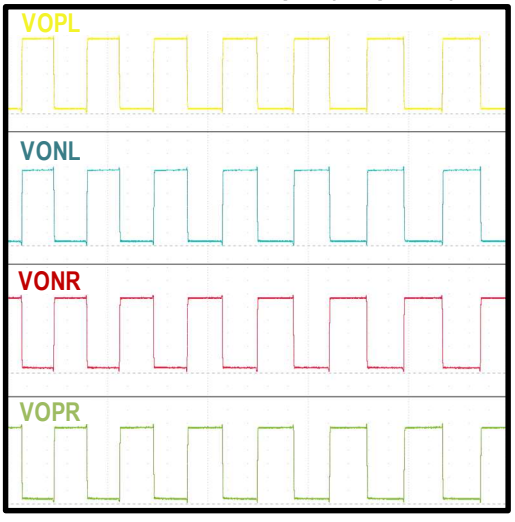
Crosstalk vs Frequency



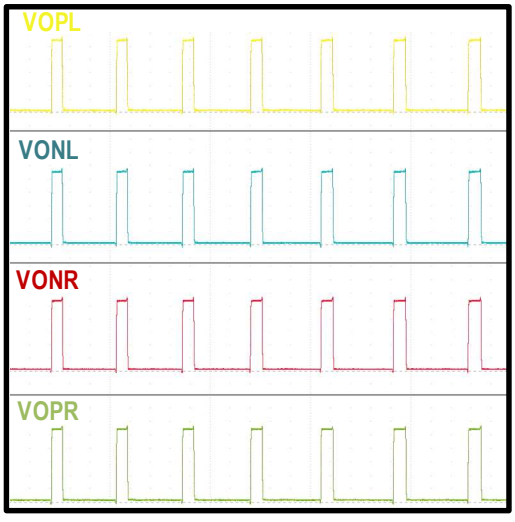
Crosstalk vs Frequency



BD Mode PWM Output (De-phase)



1SPW Mode PWM Output (In-phase)



Functional Description

The HAA3605 stereo Class-D audio amplifier features a filter-less modulation scheme that greatly reduces the external component count, conserving board space and reducing system cost. The HAA3605 does not require an output filter; it relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to recover the audio component of the square wave output.

Differential Inputs

The HAA3605 features a differential input structure, making them compatible with many CODECs, and offering improved noise immunity over a single-ended input amplifier. In devices such as flat-panel displays, noisy digital signals can be picked up by the amplifier's inputs. These signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies only the difference of the two inputs, while any signal common to both inputs is attenuated.

The HAA3605 can also be configured as a single-ended input application by AC capacity coupling either input to GND and driving the other input. It is recommended to put the ac ground input parallel with the signal input and connect to GND near the audio source which for better noise immunity.

For good transient performance, the impedance seen at each of the two differential inputs should be the same. The impedance seen at the inputs should be limited to an RC time constant of 3ms or less if possible. It allow the input dc blocking capacitors to become completely charged during the 50-ms power-up time. If the input capacitors are not allowed to completely charge, there is some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Gain Selection

The HAA3605 has 3 gain settings which can be selected by setting GAIN and AGC pins. See Table Below.

GAIN PIN	AGC PIN	Gain (dB)
GND	Floating	20
AVDD/Floating	Floating	26
GND	Other states	26
AVDD/Floating	Other states	32

The others states can be seen in *Operating Control Description*.

Internal Analog Supply (GVDD)

The HAA3605 includes an integrated low dropout (LDO) linear regulator to generate a 5 V supply which used to power the gates of the output full bridge transistors. This analog supply voltage is available at the GVDD pin. Connect a 1 μF decoupling capacitor from this pin to the GND pin. The GVDD pin is not recommended to be used as a voltage source for external circuitry.

Diagnostic SDB/FAULTB Operation

The HAA3605 features a shutdown mode that reduces power consumption. Driving SDB/FAULTB pin low places the device in low-power (10μA) shutdown mode. When device is in shutdown mode, the output of amplifier becomes weak low (a state grounded through approximately 10kΩ resistance). Connect SDB/FAULTB high for normal operation. Never leave SDB/FAULTB unconnected, because the amplifier operation would be unpredictable. For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

The SDB/FAULTB pin is also an output pin which reports protection state. When OCP, OTP, DCP is triggered, the SDB/FAULTB is activated to low level. An internal circuit will pull down it to enter shutdown mode. The pin can be connected to power supply

by a high pull-up resistor to reduce the maximum sinking current of the pin.

POP-AND-CLICK SUPPRESSION

Voltage transients at the outputs of the audio amplifiers may occur when shutdown is activated or deactivated. Voltage transients as small as 10 mV can be heard as an audible pop in the speaker. Clicks and pops are defined as undesirable audible transients generated by the amplifier system that do not come from the system input signal. Such transients may be generated when the amplifier system changes its operating mode. For example, system power-up and power-down can be sources of audible transients.

The HAA3605 features comprehensive click-and-pop suppression that eliminates audible transients on startup and shutdown. While in shutdown, the H-bridge is pulled to GND through internal resistor. During startup or power-up, the input amplifiers are muted and an internal loop sets the modulator bias voltages to the correct levels, preventing clicks and pops when the H-bridge is subsequently enabled. Additionally, well matched input capacitors and small input RC time constant can reduce this noise.

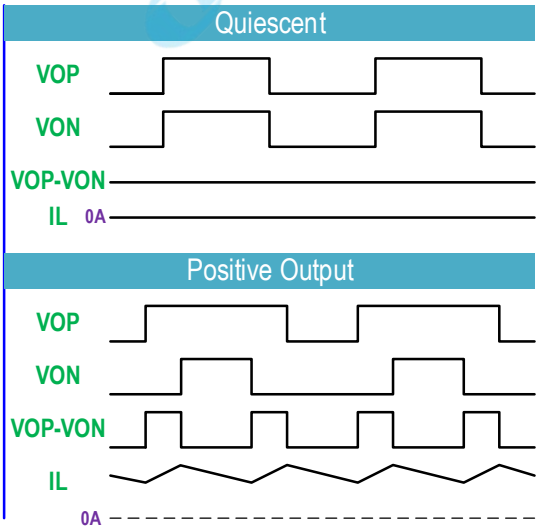
PWM Output Mode

HAA3605 has two PWM output mode. It can operate in BD Modulation or 1SPW Modulation which selected by MODE pin.

MODE PIN	Mode
GND	BD
AVDD/Floating	1SPW

BD Modulation

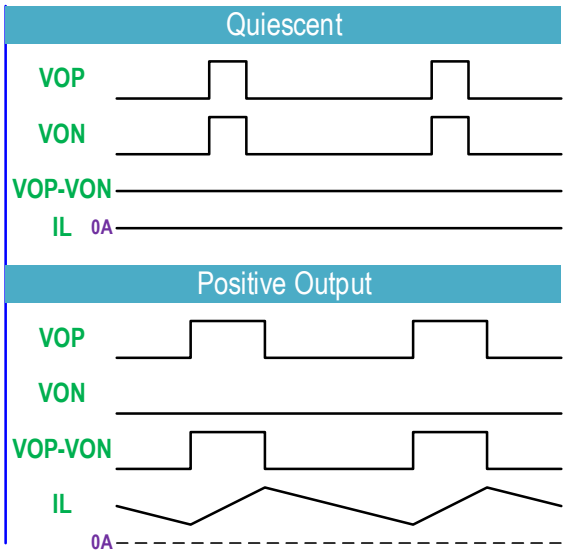
HAA3605 features PWM output signal with a carrier frequency of approximately 330 kHz, which built-in 2nd integrating loop filter to improve the THD+N performance. Each output is switching from 0 volts to the supply voltage with 50% duty cycle at quiescent state. The VOPx and VONx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of VOPx is greater than 50% and VONx is less than 50% for positive output voltages. The duty cycle of VOPx is less than 50% and VONx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.



1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~16% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching

losses. The THD penalty in 1SPW mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.



PBTL Selection (Mono Mode)

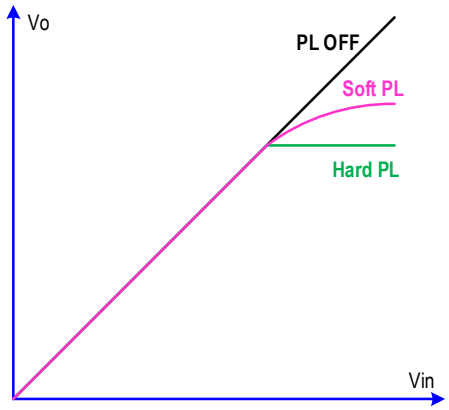
The HAA3605 features a PBTL mode that allows the right and left channels to operate in parallel, achieving up to 30W of output power with a 2Ω speaker - a particularly useful feature for driving the subwoofer in a 2.1 audio system. The PBTL mode is enabled by connecting INPL and INNL pins to GND and applying the input signal to INPR and INNR. In this mode, the positive and negative outputs of each channel (left and right) are synchronized and in phase. Speaker will be placed between the Left and Right outputs with VOPL connected to VONL and VOPR connected to VONR to parallel the output half bridges for highest power efficiency.

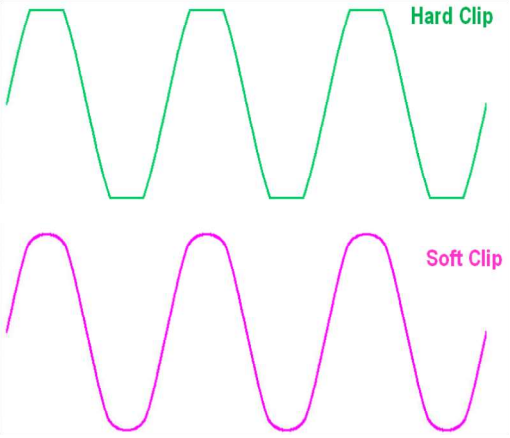
When the device is placed in PBTL mode on a PCB with outputs wired together, ensure that the INPL and INNL pins can never be driven high. Driving the INPR and INNR pins high while the outputs are wired together in PBTL mode may trigger the OCP or OTP or both, and may even damage the device.

PL (Power Limit) Function

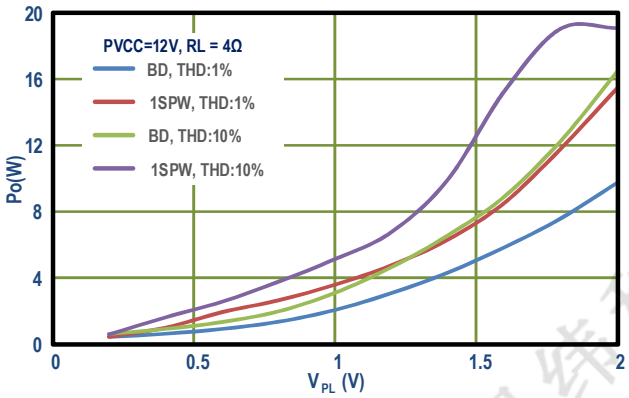
A built-in power limit is used to limit the output voltage level below the supply rail by limiting the duty cycle. Using this function protects small speakers which used in high voltage power supply, as the maximum output power can be limited. The limit level is set through the voltage (V_{PL})) at PLIMIT pin. The pin voltage is set by voltage dividing resistors from GVDD to GND. The setting values shown here are common to BTL and PBTL mode.

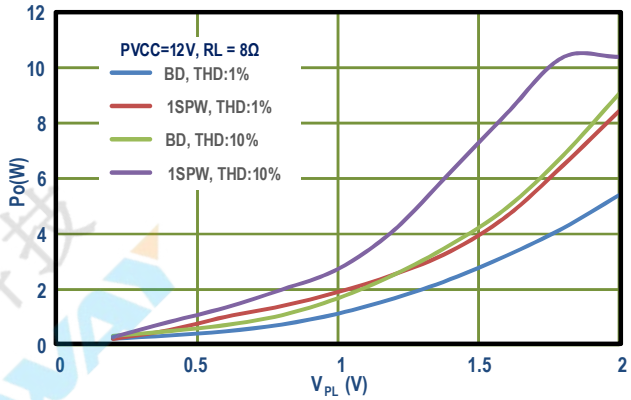
HAA3605 features soft clip power limit to reduce the harmonic distortion which has better sound quality than hard clip.





The Power limit value varies with V_{PL} voltage as shown below.



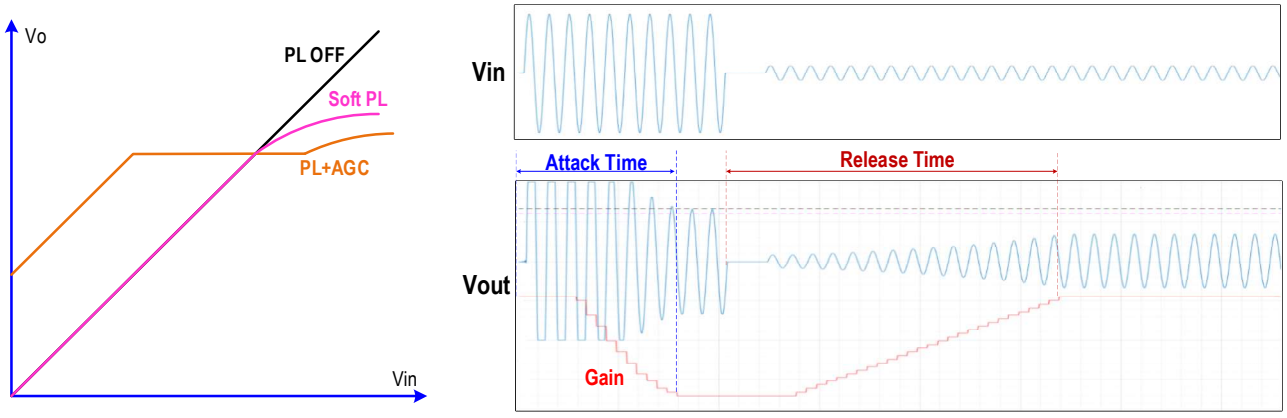


Power limit AGC Function

The HAA3605 has a built-in AGC function which works together with PL function. The AGC function can be enabled or disabled by the AGC pin as shown in *Operating Control Description*. The AGC function limits excessive output voltage to the power limit output level. When an excessive level input signal is sent to HAA3605 the AGC function will automatically reduce the amplifier gain to maintain power limit output signal to preserve high audio quality and to protect the speaker from excessive power. The AGC function works with a fast attack speed and a slower release speed to achieve maximum protection and a minimum number of audible noise. There are three sets of AGC parameters can be selected as below table. AGC1 has more loudness and AGC3 has less noise.

AGC PIN	AGC Mode	Attack Time	Release Time
GND	AGCOFF		
50kohm to GND	AGC1	60ms	600ms
100kohm to GND	AGC2	33ms	600ms
200kohm to GND	AGC3	13ms	1200ms
Floating	AGCOFF		

When the input level multiplied by the closed loop gain exceeds the limiter threshold set by the PLIMIT pin voltage, the closed loop gain is reduced in a single or by multiple 0.5dB steps until the output signal voltage gets below the level set by the PLIMIT pin voltage, or if a -12.0dB gain reduction limit is reached. When the output voltage gets below the release threshold, the closed loop gain is increased by a single or by multiple 0.5dB steps until the release threshold is reached, or the closed loop gain is at its nominal closed loop gain level.



Low EMI Noise

The HAA3605 uses a proprietary modulation and several functions to minimize EMI during playing audio. The HAA3605 can pass FCC Class-B emissions testing with unshielded 20 inch cable only using ferrite bead-based filtering.

SSM (Spread-Spectrum)

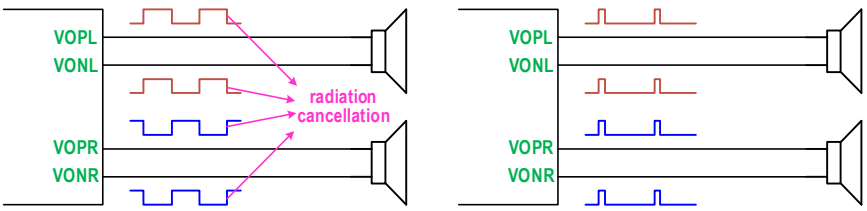
The HAA3605 features a spread-spectrum (SSM) function that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables. In SSM function, the switching frequency varies by ±10.5% around the center frequency. The period of the triangle waveform changes from cycle to cycle. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes.

AERC (Active Edge Rate Control)

The switch edge of amplifier output brings obvious EMI radiation. And the faster the edge rate, the more serious the radiation. A slower edge rate can reduce EMI radiation, but with a consequent reduction in efficiency. HAA3605 applies AERC function to the output stage, which only reduces the internal driving capacity when the edge changes. Therefore, the EMI radiation is reduced while the efficiency loss is reduced.

De-phase

The HAA3605 features de-phase function which inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity. De-phase only works with BD mode and disabled in 1SPW mode.



Protection functions

The HAA3605 is fully protected against UVP (under-voltage protection), OVP (over-voltage protection), OTP (over-temperature protection), OCP (over-current protection) and DCP (DC detection protection) as explained below.

The behavior of the device under the different fault conditions differs according to the protection activated and is described in the following sections.

UVP

This is the function to protect the device when the supply voltage is unusually lowered. If the supply voltage drops below the

UVP threshold voltage, the protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

OVP

This is the function to protect the device when the supply voltage is unusually raised. If the supply voltage exceeds the OVP threshold voltage, the protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

OTP

This is the function to prevent damage to the device when the internal die temperature exceeds the threshold temperature. If the OTP is activated, the chip is disabled until the temperature drops below the recovery threshold. This hysteresis prevents rapid cycling of the output at high temperatures. Once the die temperature exceeds the thermal triggering point, the device is switched to the shutdown state and the outputs are disabled. Thermal protection faults are reported on the SDB/FAULTB pin.

OCP

This is the function to protect the device by detecting short-circuiting conditions. If the output current exceeds the threshold value, the overcurrent protection is activated, the device is switched to the shutdown state and the outputs are disabled. The device will recover automatically when the fault is removed. Over-current protection faults are reported on the SDB/FAULTB pin.

DCP

This is the function to protect the speaker connected to the amplifier output when a DC signal is continuously output. The DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the SDB/FAULTB pin as a low state and switch the device to shutdown state. The device will recover automatically when the fault is removed.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds approximately22% (for example, +61%, -39%) for more than 800ms at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SDB/FAULTB pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Application Information

The HAA3605 features SSM, AERC, De-phase functions to remove the inductor filter in applications like as TV sets, sound docks and Bluetooth speakers. Depending on output power requirements and necessity for load protection, the built in PL function can be used to control system power, see functional description of this feature.

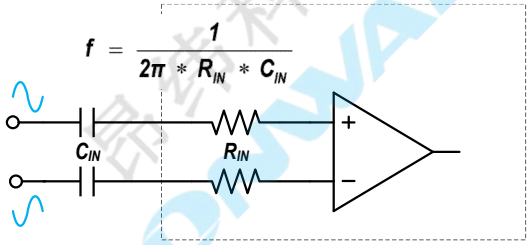
Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVCC pin is decoupled with ceramic capacitors placed as close as possible to each supply pin. It is recommended to follow the PCB layout Description below.

Input Filter (Input Capacitor Selection)

The input impedance is set by an internal resistor which is selected by gain setting. As shown below.

Gain (dB)	Rin_int (kΩ)
20	40
26	20
32	10

An input capacitors are required if the input signal is not biased within the recommended input dc common-mode voltage range. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the HAA3605 form a high-pass filter with a corner frequency determined by the following figure.



For Gain=26dB and C_{IN}=0.22μF, the high pass cutoff frequency is about 36Hz. A further consideration for this capacitor is the leakage path from the input source through the input network and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

The input capacitor should be match well and can significantly affect the performance of the circuit. Failure to use input capacitors degrades the output offset of the amplifier.

Bootstrap Capacitors

The output stage of the HAA3605 uses a high-side NMOS driver, rather than PMOS driver. To generate the gate drive voltage for the high-side NMOS driver, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Using 0.22 μF ceramic capacitors with a voltage rating of 25 V or greater is recommended.

For a properly functioning bootstrap circuit, the ceramic capacitor must be closed to each bootstrap pin and the power-stage output pin. When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. These capacitors ensure sufficient energy storage, even during clipped low frequency audio signals, to keep the high-side

power stage FET (nLDMOS) fully turned on during the remaining part of its ON cycle.

Power Supply Decoupling

To ensure high efficiency, low total harmonic distortion, and high power supply rejection ratio, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. Decouple the power supply input with a good quality aluminum electrolytic capacitors larger than 220μF that are placed on the power supply of each channel. This capacitor bypasses low frequency noises to the ground plane which serves as a local storage capacitor for supplying current during large signal transients from the speaker. For high frequency transient noises, good quality low ESR and ESL ceramic capacitors typical 1μF and 1nF should be placed as close as possible to the power supply of each channel. A 1μF ceramic capacitor should be placed on the AVCC pin and a small resistor between AVCC and PVCC can be used to keep high frequency noise from entering the analog circuit. 25V capacitor rating is recommended.

Output Filter

The HAA3605 does not require an output filter. However, output filtering can be used if a design is failing radiated emissions due to board layout or cable length, or the circuit is near EMI-sensitive devices. The tuning and component selection of the filter should be optimized for the load.

Ferrite Bead Filter

Several emissions suppression technology are used in HAA3605 eliminates the need for expensive LC filter. Low-cost ferrite bead-based filters can meet the requirements. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1nF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

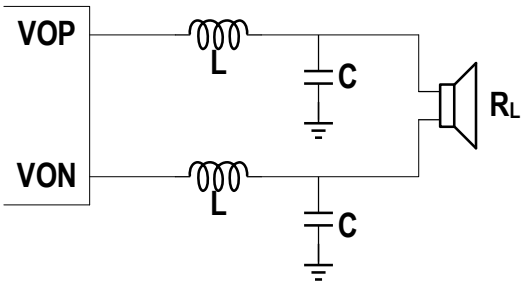
Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead's current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than 50% under this condition is desirable.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND or the thermal pad beneath the chip.

LC Filter

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter should be used shown below. The recommended component values are listed in the table below. Using these constants makes a cut-off frequency from 20 kHz~50 kHz with Q ≈ 0.7.



$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$Q = \frac{R_L}{2}\sqrt{\frac{C}{L}}$$

R_L (Ω)	L (μH)	C (μF)	f (kHz)	Q
8	33	1	27.7	0.7
8	22	0.68	41.2	0.7
6	22	1	33.9	0.64
6	15	1	41.1	0.77
6	10	0.68	61	0.78
4	15	2.2	27.7	0.77
4	10	1	50	0.63
4	10	0.68	61	0.52

PCB Layout Considerations

As output power increases, it must take care to layout PCB traces and wires properly among the amplifier, load, and power supply; a poor layout increases voltage drops, consequently decreasing efficiency. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground.

To maintain high output swing and high peak output power, ensure that the PCB traces that connect the output pins to the load and supply pins are as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances. Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna. In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

The ferrite-bead filter or LC filter should be placed as close to the output pins as possible for the best EMI performance. The capacitors used in both the ferrite-bead and LC filters should be grounded to power ground. In addition, properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate ground planes for small signal and high power connections, there should be no overlap between these planes. Stitch the power plane to the exposed Thermal pad using multiple vias. Proper layout improves heat conduction into the board, allowing operation at larger output power levels without over-temperature issues.

PCB Material Recommendation

FR-4 Glass Epoxy material with 1 oz. (35 μm) is recommended. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance). It is recommended to use several GND underneath the device thermal pad for thermal coupling to a bottom side copper GND plane for best thermal performance.

Thermal Considerations

Class D amplifiers provide much better efficiency and thermal performance than a comparable Class AB amplifier. However, the system's thermal performance must be considered with realistic expectations along with its many parameters.

- **Crest factor (Continuous Sine Wave vs. Music)**

Crest factor is the ratio of the instantaneous peak amplitude of a waveform, to its root mean square RMS value. Typically music has a crest factor of 10 to 20dB and the sine wave is 3dB. When a Class D amplifier is evaluated in the lab, often a continuous sine wave is used as the signal source. While this is convenient for measurement purposes, it represents a worst-case scenario for thermal loading on the amplifier. It is not uncommon for a Class D amplifier to enter thermal shutdown if driven near maximum output power with a continuous sine wave. The PCB must be optimized for best dissipation.

Audio content, both music and voice, has a much lower RMS value relative to its peak output power. Therefore, while an audio signal may reach similar peaks as a continuous sine wave, the actual thermal impact on the Class D amplifier is highly reduced. If the thermal performance of a system is being evaluated, it is important to use actual audio signals instead of sine waves for testing. If sine waves must be used, the thermal performance is less than the system's actual capability for real music or voice.

- **PCB Thermal Considerations**

The exposed pad is the primary route for conducting heat away from the IC. With a bottom-side exposed pad, the PCB and its

copper becomes the primary heat-sink. Solder the exposed pad to a copper polygon. Add as much copper as possible from this polygon to any adjacent pin on the Class D amplifier as well as to any adjacent components, provided these connections are at the same potential. These copper paths must be as wide as possible. Each of these paths contributes to the overall thermal capabilities of the system.

The copper polygon to which the exposed pad is attached should have multiple hot solid vias to the opposite side of the PCB, where they connect to another copper polygon. Make this polygon as large as possible within the system's constraints for signal routing. Additional improvements are possible if all the traces from the device are made as wide as possible. Although the IC pins are not the primary thermal path out of the package.

- **Heat-sink requirements**

If operating in higher ambient temperatures, it is possible to improve the thermal performance of a PCB with the addition of an external heat-sink. The thermal resistance to this heat-sink must be kept as low as possible to maximize its performance. With a bottom-side exposed pad, the lowest resistance thermal path is on the bottom of the PCB. Placing heat-sink on the back of the PCB which under the device will bring obvious effects. But it will bring some structural problem in the design. Sometime, attaching heat-sink to the topside of the device with thermal conductive silicone is more appropriate.

- **Thermal Calculations**

The die temperature of a Class D amplifier can be estimated with some basic calculations. For example, the die temperature is calculated for the below conditions:

T_A = +35°C, P_{OUT} = 2x10W, η = 92.5%, θ_{JA} = 30.3°C/W

Then, the Class D amplifier's power dissipation can be calculated:

$$P_{DISS} = \frac{P_{OUT}}{\eta} - P_{OUT} = 1.622W$$

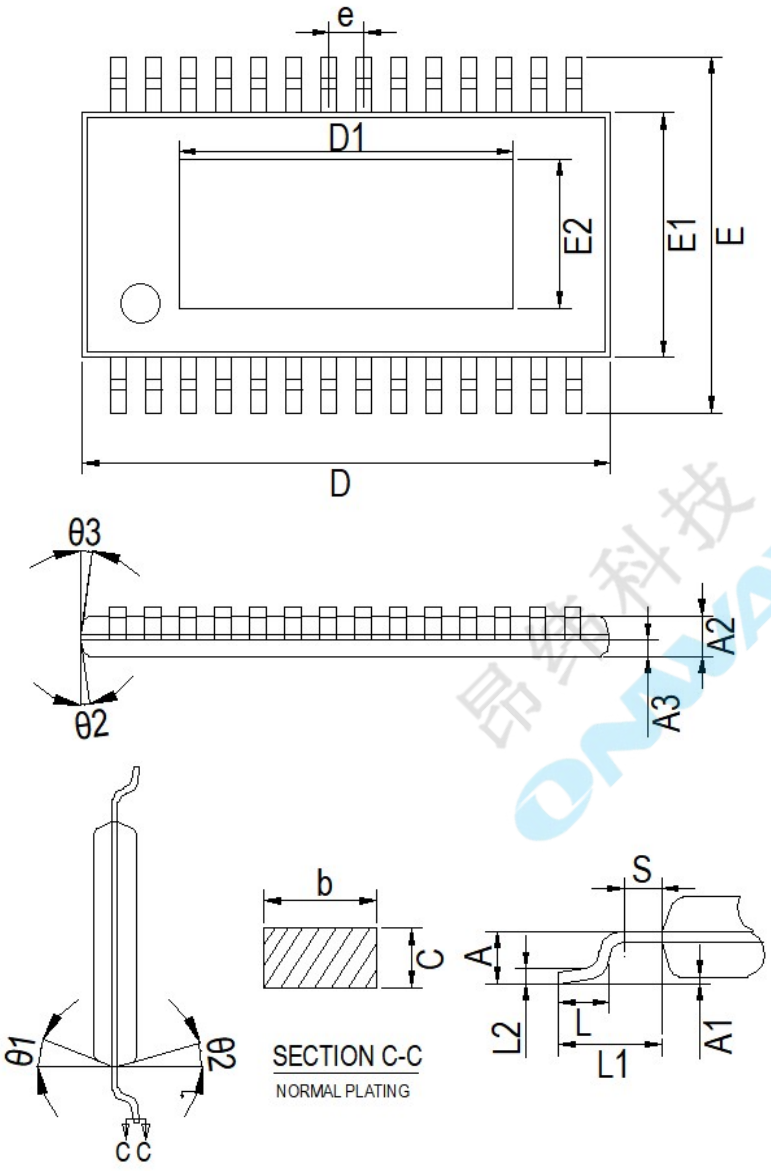
Then the die temperature can be calculated:

$$T_C = T_A + P_{DISS} * \theta_{JA} = 84.15℃$$

Package Outline

ETSSOP-28L

Plastic thermal enhanced thin shrink small outline package, 28 leads.
Body width 4.4 mm, body length 9.7mm, lead pitch 0.65 mm, exposed die pad.



COMMOV DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
SYMBOL	MIN	NOM	MAX
A	-	-	1.2
A1	0.05	-	0.15
A2	0.90	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.29
c	0.13	-	0.18
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
S	0.20	-	-
Θ1	10°	12°	14°
Θ2	10°	12°	14°
Θ3	10°	12°	14°
Θ4	10°	12°	14°
Exposed Thermal PAD			
D1	3.4		6.4
E2	2.5		2.9

Revision History

No	Date	Description
V1.0	20221028	First release