SiI9612 4K Video Processor with Integrated 300 MHz Receiver and Transmitter

Data Sheet

SiI-DS-1120-C

April 2017

Contents

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1. General Description

The Lattice Semiconductor SiI9612 video processor supports High-definition Multimedia Interface (HDMI®) and video processing requirements for a Blu-ray Player/Recorder, Audio Video Receiver (AVR), and other video processors. It incorporates an integrated HDMI/Mobile High-definition Link 2 (MHL®) receiver and an HDMI transmitter that supports HDCP repeaters.

Lattice Semiconductor VRS® ClearView video processing enhances video streaming quality with noise reduction, Video Smoothing™, and picture enhancement. VRS® ClearView also includes a 4K adaptive scaler to drive the emerging 4K display market.

The SiI9612 device is preprogrammed with High-bandwidth Digital Content Protection (HDCP) keys for both receiver and transmitter, which helps reduce programming overhead and lowers manufacturing costs.

1.1. Video Processor

- Supports video input formats up to 1080p and UXGA including 4K x 2K pass-through
- Supports video output formats up to 1080p, WUXGA, and 4K x 2K
- Full 10-bit Adaptive Scaler
- Mosquito Noise Reduction
- Supports upscaling to 4K x 2K
- Supports downscaling from 1080p @ 60 Hz
- Video smoothing (pre- and postscaler)
- Detail and edge enhancement (prescaler)
- 12-bit preprocessing including color space conversion and picture control
- 12-bit postprocessing including color space conversion
- Picture controls
- Test Pattern Generator (TPG)

1.2. On-screen Display

- Character-based
- Supports On-screen Display (OSD) over 3D video
- Supports alpha-blending

1.3. Video Input

- 300 MHz HDMI receiver port with 3D support
- MHL with 1080p @ 60 Hz support

1.4. Video Output

- 300 MHz HDMI transmitter port

1.5. Digital Audio Interface

- Inputs
  - I^2S input with multichannel support
  - S/PDIF input
  - Audio Return Channel (ARC) input
- Outputs
  - I^2S output with four data signals for multichannel formats, and flexible programmable channel mapping including DSD
  - High Bitrate Audio output including Dolby® TrueHD and DTS-HD Master Audio™
  - S/PDIF output supports LPCM, Dolby Digital, DTS digital audio transmission with a 32 kHz – 192 kHz f_S sample rate
- Intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute
- IEC60958 or IEC61937 compatible

1.6. Control

- I^2C and Serial Peripheral Interface (SPI) Bus
- DDC for HDMI receiver and transmitter
- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O and an integrated CEC Programming Interface (CPI)

1.7. Package

- 9 mm × 9 mm, 76 pin MQFN package with ePad

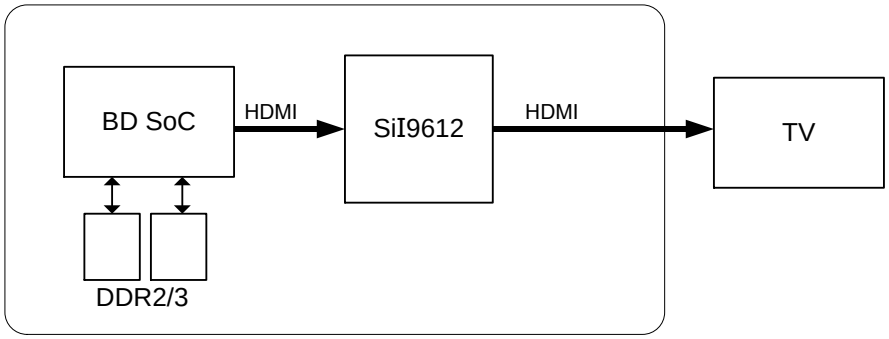

Figure 1.1. Typical Application

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2. Functional Description

The SiI9612 video processor is ideally suited for Blu-ray players, A/V receivers, and video processing applications. It features a digital processing core that performs real-time video format conversion and image improvement. Format conversion is achieved through an innovative adaptive scaler that allows the device to upscale from any input format to 4K x 2K resolutions. Proprietary video processing algorithms improve the picture quality by removing unnaturally appearing noise or artifacts, smoothing edges and sharpening the image. Image improvement is supported for both standard and high-definition video.

An on-chip character generated On-screen Display (OSD), organized as 108 x 30 rows and columns, is included in the SiI9612 device. The OSD has split-screen mode to support display of the OSD over a 3D image.

The SiI9612 device provides a Test Pattern Generator (TPG) that is fully programmable by software and is able to generate test patterns without a valid input signal. With a maximum supported resolution of 4096 x 2208, it is able to generate test patterns for both 4K x 2K and 1080p 3D video output formats.

The SiI9612 video processor integrates a full 300 MHz HDMI receiver and HDMI transmitter. Mobile High-definition Link (MHL) technology is available on the HDMI receiver. The MHL receiver supports PackedPixel mode. The Audio Return Channel (ARC), provided for the HDMI transmitter port, allows the SiI9612 device to receive a S/PDIF signal from the connected DTV.

The SiI9612 video processor supports audio extraction and insertion. Audio extracted from the HDMI receiver can be output simultaneously to a S/PDIF port, a multichannel I^2S port, and to the HDMI transmitter for repacketization. Audio to be transmitted on the HDMI output can be selected from one of four other sources: S/PDIF input, 2-channel I^2S input, multichannel I^2S input, and ARC input. The video processor can also convert the LPCM data received from the 2-channel I^2S input or the I^2S output of the HDMI receiver to an IEC60958 stream to output on the S/PDIF port.

Figure 2.1 below and Figure 2.2 on the next page show the functional blocks of the chip.

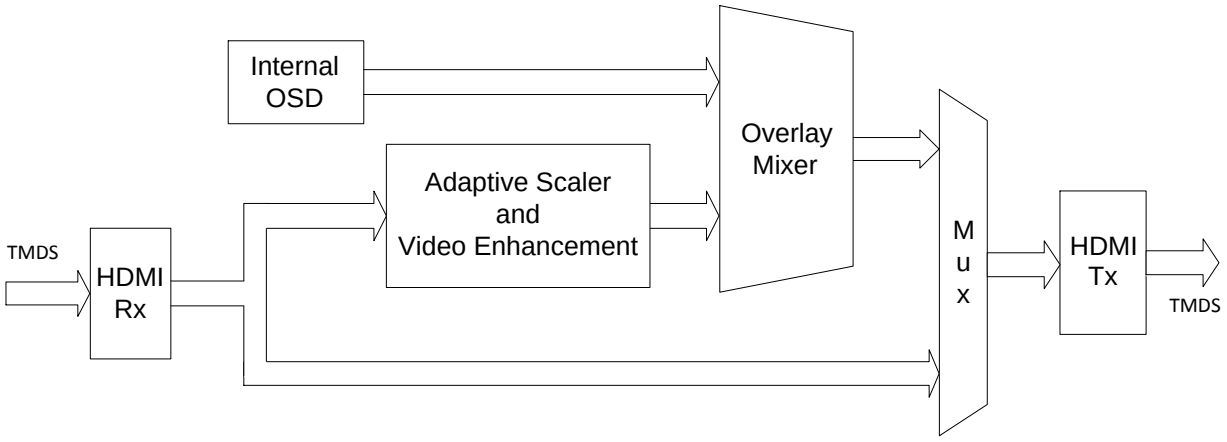

Figure 2.1. Functional Video Path Block Diagram

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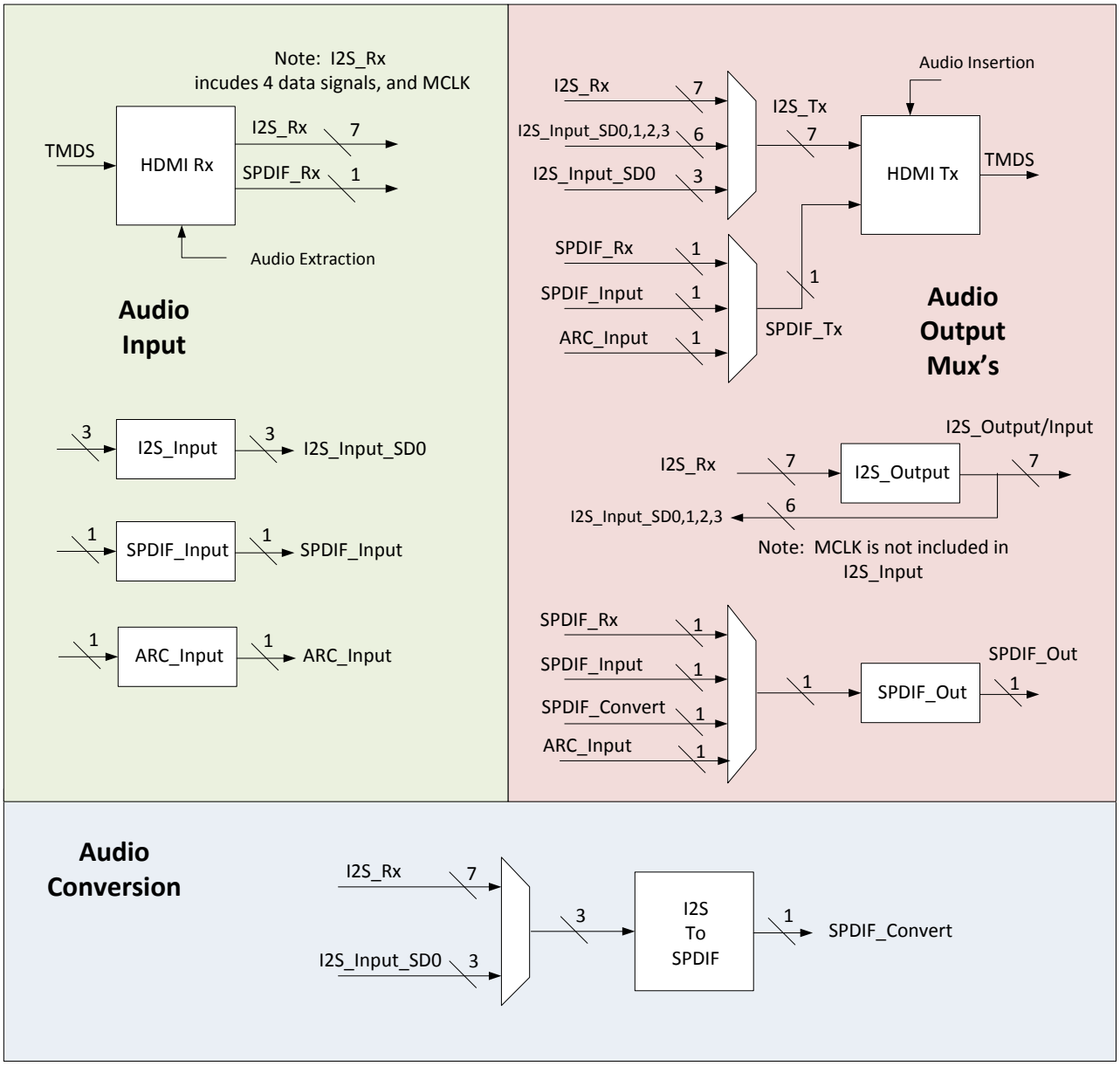

Figure 2.2. Audio Path Block Diagram

Table 2.1 summarizes the audio outputs that are available with each audio input.

Table 2.1. Audio Multiplexing Options

Audio Input	Audio Output			
	SPDIF_Out	I2S_Output	HDMI SPDIF_Tx	HDMI I2S_Tx
SPDIF_Input	Supported	—	Supported	—
I2S_Input	Supported (2-channel formats)	Supported	—	Supported
HDMI SPDIF_Rx	Supported	—	Supported	—
HDMI I2S_Rx	Supported (2-channel formats)	Supported	—	Supported
ARC_Input	Supported	—	Supported	—

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2.1. Video Processor

The SiI9612 video processor features the latest VRS® technologies from Lattice Semiconductor including a 4K Adaptive Scaler, Video Smoothing, enhanced Mosquito Noise Reduction, and Detail and Edge Enhancement. These technologies improve the picture quality of highly compressed video sources by enhancing resolution through scaling and removing video noise without side effects. Adaptive scaling delivers automatically optimized performance for all sources including internet video, high-definition video, and computer graphics. All processing resources are included on-chip and external RAM is not required.

2.1.1. Supported Input Resolutions to Video Processing Core

The SiI9612 video processing core supports several input formats as defined in the CEA-861E Specification. It also supports several PC formats. Supported formats include, but are not limited to, the following:

- 720 x 480i
- 720 x 576i
- 1440 x 480i
- 1440 x 576i
- 720 x 480p
- 720 x 576p
- 1280 x 720p50
- 1280 x 720p60
- 1920 x 1080i50
- 1920 x 1080i60
- 1920 x 1080p50
- 1920 x 1080p60
- VGA
- SVGA
- XGA
- SXGA
- UXGA
- 4K x 2K @ 23.98 Hz, 24 Hz, 25 Hz, 29.97 Hz, and 30 Hz pass-through
- 4K x 2K YCbCr 4:2:0 @ 59.94 Hz, 60 Hz, and 50 Hz pass-through

1080p resolutions may require a small amount of vertical zoom when scaling down to certain SD resolutions.

The SiI9612 video processor does not support frame rate conversion. The output frame rate always needs to be the same as the input frame rate.

2.1.2. Special Considerations for 4K x 2K Inputs

4K x 2K inputs must bypass all major processing blocks. In this mode, color space conversion and picture controls are still available. The exception is YCbCr 4:2:0 encoded 4K x 2K @ 60 Hz (59.94 Hz) and 50 Hz inputs, in which color space conversion and picture controls must also be bypassed.

Figure 2.4 on page 12 shows the bypass modes available on the SiI9612 video processor.

2.1.3. Supported Output Resolutions

The SiI9612 video processing core supports several output formats including the following:

- 480i
- 480p
- 576i
- 576p
- 720p
- 1080i
- 1080p
- VGA
- SVGA
- XGA
- SXGA
- UXGA
- 4K x 2K @ 23.98 Hz, 24 Hz, 25 Hz, 29.97 Hz, and 30 Hz
- 4K x 2K YCbCr 4:2:0 @ 59.94 Hz, 60 Hz, 50 Hz

The SiI9612 device does not support frame rate conversion. The output frame rate always needs to be the same as the input frame rate.

2.1.4. Video Processing Blocks

The SiI9612 video processor contains the following video processing blocks:

- Input Preprocessing reformats the input signal to YCbCr 4:2:2 format
- Mosquito Noise Reduction
- Standard Definition Edge Smoothing
- High-definition Detail and Edge Enhancement
- Adaptive Video Scaling
- High-definition Edge Smoothing
- Test Pattern Generation
- Internal OSD Blending
- Output Postprocessing reformats the video data to many different output formats

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Figure 2.3 shows a block diagram indicating the placement of these blocks in the video path.

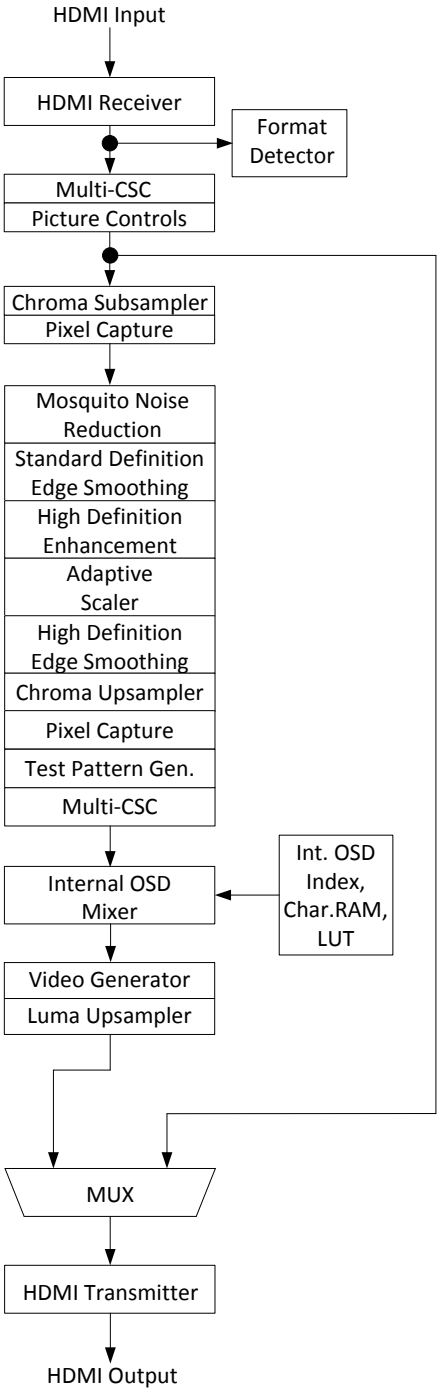

Figure 2.3. Video Processing Blocks

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2.1.5. Bypass Modes

The SiI9612 device provides two options for bypassing the internal processing blocks using control registers that are described in the SiI9612 programmer's reference (*SiI-PR-1069; requires NDA with Lattice Semiconductor*). Figure 2.4 shows the available bypass options.

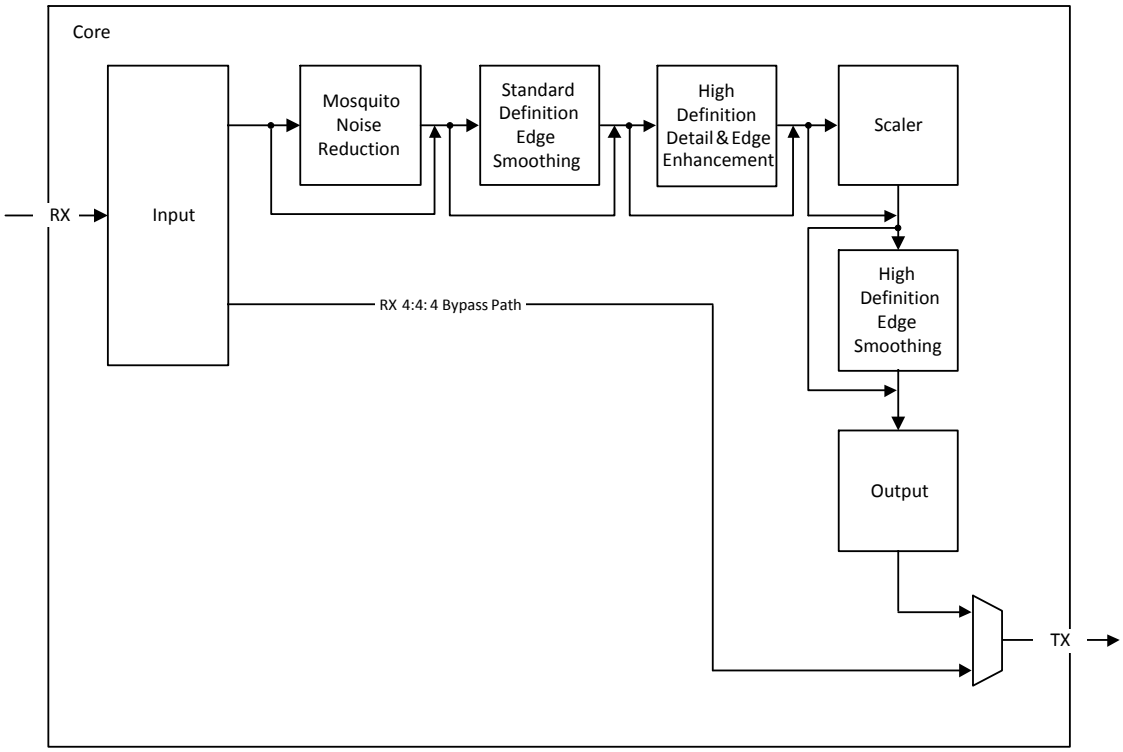

Figure 2.4. Bypass Options

2.1.6. Processing Mode

In processing mode, the output of the SiI9612 video processor can be in RGB or YCbCr mode. Multiple color space converters, chroma upsampler, and chroma downsampler logic blocks are available on the input and output of the processing block to ensure support for a wide range of applications.

2.2. Input Preprocessing

The SiI9612 video processor provides a number of video processing functions that can be used to adjust the incoming video signal before it is sent to the scaler and enhancement blocks. These functions are color space conversion, picture controls, and chroma subsampling. All processing is done in 36 bits.

2.2.1. Picture Controls

Picture controls are used to adjust the following aspects of the video input signal:

- Input Black Level: 4096 levels of black level control.
- Contrast: 1 integer bit, 8 fractional bits. Range is from 0 to 1.996 with a 1/256 resolution for a total of 512 levels of contrast control.
- Saturation:1 integer bit, 8 fractional bits. Range is from 0 to 1.996 with a 1/256 resolution for a total of 512 levels of saturation control.

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2.2.2. 3 x 3 Matrix (Multicolor Space Converter)

In addition to the built-in picture controls, the SiI9612 device features a 3 x 3 matrix module at the input path. These can be used as programmable linear control to adjust the brightness, contrast, saturation, and hue in the three components of the input signal. It can also be used to perform RGB-to-YCbCr and YCbCr-to-RGB color space conversions.

The 3x3 matrix also comes with 64 sets of predefined coefficients to support all standard color space conversions.

Table 2.2 shows the eight possible formats available for the input and output of the 3 x 3 matrix.

Table 2.2. Multicolor Space Converter Input/Output Formats

Color Space	Levels	Colorimetry
YCbCr	Video	709
YCbCr	Video	601
YCbCr	PC	709
YCbCr	PC	601
RGB	Video	709
RGB	Video	601
RGB	PC	709
RGB	PC	601

2.2.3. Chroma Subsampler

The chroma subsampler module converts YCbCr 4:4:4 input signals to YCbCr 4:2:2 format.

2.3. Mosquito Noise Reduction

The SiI9612 video processor detects and removes mosquito noise. Mosquito noise is a common compression artifact caused by MPEG decoders, and is often exhibited around the edges of text and computer generated graphics. The SiI9612 algorithm detects areas where mosquito noise would be the most likely, and then works to diminish the mosquito noise without blurring the edge of the text or graphic. The maximum resolution supported by mosquito noise reduction is 576p.

2.4. Video Smoothing

The Lattice Semiconductor Video Smoothing technology removes the rough edges in an image, such as the staircase appearance of a diagonal line drawn on the screen without edge smoothing (stair stepped effect). Digital compression, scaling artifacts, poor quality deinterlacing, or resolution limitations in the digital sampling of an image cause these effects. Smoothing technology creates the effect of a high resolution image without softening the entire image.

The SiI9612 device offers two smoothing blocks. The Standard Definition Edge Smoothing block comes before the scaler block and removes any rough edges on the original image. The High-definition Edge Smoothing block comes after the scaler and it reduces rough edges caused by upscaling the video.

2.5. Detail/Edge Enhancement

There are two types of sharpening in the SiI9612 device: general and edge-qualified. Sharpening is done before scaling in the High-definition Enhancement block. The High-definition Enhancement block works well for sharpening both SD and HD video.

Detail enhancement can be used to increase fine detail or reduce noise for overly enhanced images. Detail enhancement is controlled with an 8-bit signed register. Positive control numbers from 1 to 127 increase sharpening and negative numbers in two's complement format decrease sharpening. This means that if the control word is negative, the image is low-pass filtered. The control register defaults to 0, which does not apply any sharpening.

Edge enhancement can be used to sharpen edges or reduce overly enhanced edges. The edge qualified sharpening or edge enhancement works only on object edges. It also uses an 8-bit signed control word, like general sharpening, so

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sharpening can increase around object edges if the control word is positive, and edges of objects can be filtered if the control word is negative. There is a *clipping* control for edge-qualified sharpening that allows for adjustment of edge sensitivity. The clipping control is also an 8-bit number, but it is unsigned. The clipping control allows the user to select the strength of object edges to which sharpening is applied.

The detail enhancement and edge-qualified enhancement methods are additive, so the results of both sharpening methods are combined.

An example of this would be to use general sharpening to increase detail in the entire image. If object edges are overenhanced, then negative edge qualified sharpening is applied to reduce the overenhancement of the edges.

If general sharpening is applied to a noisy image, the increase in noise may be objectionable. In that case, positive edge qualified sharpening should be applied to sharpen object edges, but not increase the noise level.

2.6. Scaler

The scaler provides format conversion capability to the SiI9612 video processor. It reads the input data from internal line memory and applies horizontal and vertical scaling. Adaptive scaling ensures that the converted format is free of ringing artifacts regardless of content, whether video, graphic, or a mix of both. Format conversion is supported for both video and PC formats.

The scaler does not support a frame buffer. The output frame rate is locked to the input frame rate. A small amount of vertical zoom is necessary when scaling down from 1080p resolutions to some SD resolutions such as 480p.

The scaler can perform scaling on a limited set of Frame Packed 3D formats. The only 3D format conversions that work are conversions from 720p Frame Packed to 1080p Frame Packed, or from 1080p Frame Packed to 720p Frame Packed.

The scaler supports panorama mode that changes the aspect ratio of the image. It can be used to fit a 4:3 SD image into a 16:9 HD format with minimal distortion. This is achieved by keeping the original image aspect ratio in the center of the scaled image, and gradually stretching the image towards its left and right edges. This results in no distortion at the image center while horizontal distortion gradually increases towards the left and right edges of the image. The panorama mode features an enhanced algorithm that reduces the distortion at the far edges of the image.

The scaler also includes both a border generator and a mask generator. The border generator is used to create a grey frame about the video image whereas the mask generator can be used to create a black frame around the border. Borders provide another method for correcting the aspect ratio of the displayed image, such as displaying a 4:3 image on a 16:9 frame without horizontal distortion by adding appropriately sized pillars on the left and right side of the image.

Other functions supported by the scaler block include Y/C delay that allows a horizontal offset between the chroma and luma signal to compensate for delay differences caused by other parts of the system, automatic Chroma Upsampling Error (CUE) correction, which detects chroma data that has been upsampled incorrectly in the vertical direction and suppresses the visual artifacts caused by these errors, and user-defined zoom and pan functions.

Scaler processing is done in YCbCr 4:2:2, 20-bit (10 bits per component) color space format.

2.7. Keystoning

The SiI9612 device supports Keystoning. Keystoning is necessary when an image is projected onto a surface at an angle resulting in a distorted image of a trapezoid. For example, if a projector is lower than the surface onto which it is projecting, the image is larger at the top than at the bottom.

2.8. Standalone Video Timing Generators

The SiI9612 device features a standalone Video Timing Generator (VTG) which allows it to generate a solid colored screen with any output format supported by the device. For example, a 1080p signal which produces a solid blue screen can be output when there are no inputs to the video processor.

The input clock for the VTG can be selected from among these clock sources: 27 MHz system clock, HDMI input clock and internal video PLLs.

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2.9. Test Pattern Generator

The SiI9612 video processor has a programmable Test Pattern Generator (TPG). The TPG is flexible and under software control. It is able to generate test patterns without a valid input signal. The maximum output resolution of the TPG is 4096 x 2208. The 4096 horizontal resolution supports all 4K x 2K formats. The 2208 vertical resolution supports Frame Packed 3D formats up to 1080p.

The TPG operates in YCbCr 4:4:4 color space format at 12 bits per color component.

2.10.On-screen Display

The SiI9612 video processor comes with a built-in character-based On-screen Display (OSD). The OSD is organized as a 108 x 30 character map that can be positioned anywhere on the screen. 384 characters can be created at 12 x 24 pixels per character or 192 characters at 24 x 24 pixels per character. The OSD can support transparency and a maximum of 64 pairs of foreground and background colors. The maximum resolution of the OSD is 1296 x 720 pixels.

The OSD supports a split mode that allows it to be overlaid onto some 3D video formats. The OSD can be split vertically or horizontally. When split vertically the OSD can be overlaid onto Frame Packed 3D formats or Top-and-Bottom 3D formats. When split horizontally, the OSD can be overlaid onto Side-by-Side 3D formats. However, 3D processing downstream from the SiI9612 device of Side-by-Side (Half) and Top-and-Bottom formats will distort the characters as they will be expanded by 2x horizontally in a Side-by-Side (Half) format, or they will be expanded by 2x vertically in a Top-and-Bottom format.

2x, 3x, and 4x pixel and line replication are supported for increasing the size of the OSD characters. Pixel replication is independent for horizontal and vertical. Pixel and line replication may be used to increase the legibility of the OSD for 4K x 2K output.

The OSD is rendered in YCbCr 4:4:4 or RGB color space.

2.11.Output Postprocessing

Additional processing can be performed on the output data after the scaling/enhancement data path before it is sent to the HDMI transmitter. These functions are color space conversion and chroma upsampling. All processing is done in 36 bits.

2.11.1. Chroma Upsampler

The chroma upsampler module converts YCbCr 4:2:2 input signals to YCbCr 4:4:4 format.

2.11.2. 3 x 3 Matrix (Multicolor Space Converter)

The 3 x 3 matrix module is the same as the one in the input path. It performs color space conversion using a user-programmed coefficient and offset values, or 64 predefined sets of coefficients for all standard color space conversions.

2.12.4:2:0 Output

The SiI9612 video processor supports YCbCr 4:2:0 ready displays. The primary purpose of this pixel encoding format is to support the transmission of 4K x 2K @ 50/60 Hz formats using a link clock rate that is half the pixel clock rate, or 297 MHz, by reducing the bandwidth through chroma subsampling.

In YCbCr 4:2:0 format, the chroma components, Cb and Cr, are subsampled both horizontally and vertically with respect to the Y component by a factor of two. This produces a Y-to-Cb/Cr ratio of 4:1, which results in half the bandwidth of YCbCr 4:4:4 format. As shown in Figure 2.5 on the next page, the subsampled Cb and Cr components are co-sited and aligned with Y horizontally, but are shifted by half a line vertically.

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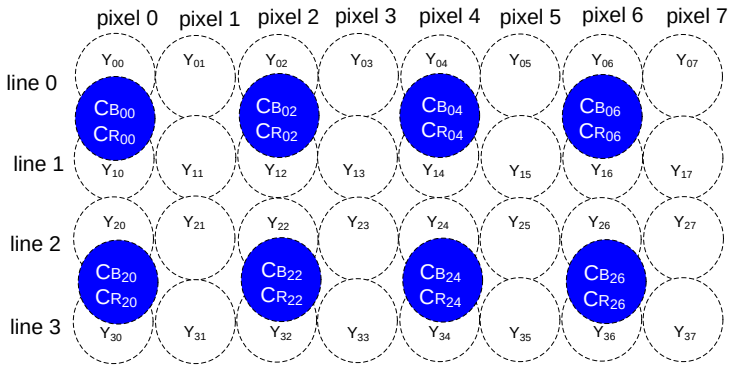

Figure 2.5. Location of Cb/Cr with Respect to Y in YCbCr 4:2:0

Figure 2.6 illustrates the organization and timing of the Y, Cb and Cr samples when transported across the HDMI link in YCbCr 4:2:0 format. Two horizontally successive Y samples are transmitted in TMDS channel 1 and 2 in order, respectively. The Cb and Cr samples are transmitted on alternate lines in TMDS channel 0, with Cb being transferred first.

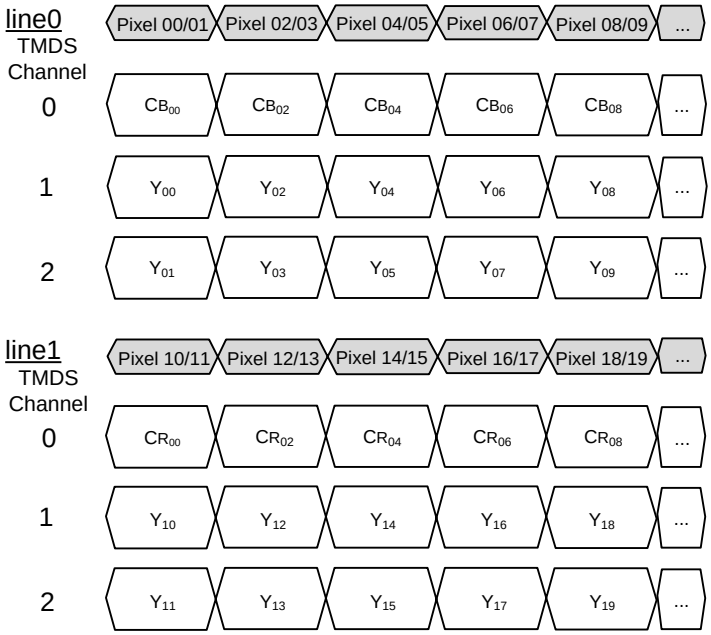

Figure 2.6. YCbCr 4:2:0 Signal Mapping and Timing Diagram

The SiI9612 video processor provides a special mode for scaling any input format with 50/60 Hz frame rate to 4K x 2K @ 50/60 Hz in 4:2:0 output format. In this mode the scaler is configured to scale the input vertically to the full 4K x 2K vertical resolution of 2160 lines and horizontally to half the horizontal resolution, either 1920 or 2048 pixels. A half line vertical shift is then applied to the chroma component of the generated signal before being upsampled by a factor of two. The resultant 4:4:4 signal then goes to a luma upsampler module where the luma component is upsampled to create two times the number of samples. In the final stage, the luma component is sent out in two pixels per clock while the chroma components Cb and Cr are clocked out on alternating lines. All processing is done with an output clock of 297 MHz.

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2.13.HDMI Output

The SiI9612 video processor features an HDMI transmitter with 300 MHz TMDS core for 1080p @ 60 Hz 3D and 4K x 2K outputs, full digital video and audio pipelines, integrated HDCP keys and encryption engine, and Audio Return Channel (ARC) input.

2.13.1. TMDS Transmitter Core

The TMDS transmitter core performs 8-bit-to-10-bit TMDS encoding on the data received from the HDCP XOR mask, and is then sent over three TMDS data and one TMDS clock differential lines. See the HDCP Encryption Engine/XOR Mask on page 17 for more details.

The transmitter core supports link clocks from 25 MHz to 300 MHz. The internal PLL has the option to multiply the pixel clock to implement deep color or pixel repetition modes.

2.13.2. Deep Color Support

The SiI9612 video processor provides support for deep color video data up to the maximum specified link speed of 3 Gb/s (300 MHz internal clock rate for the deep color packetized data). It supports 30-bit and 36-bit video input formats, and converts the data to 8-bit packets for encryption and encoding for transferring across the TMDS link.

When the input data width is wider than desired, the device can be programmed to dither or truncate the video data to the desired size. For example, if the input data width is a 12 bits per pixel component, but the sink device only supports 10 bits, the HDMI transmitter can be programmed to dither or truncate the 12-bit input data to the desired 10-bit output data.

2.13.3. Source Termination

TMDS transmitters use a current source to develop the low-voltage differential signal at the receiver end of the DC-coupled TMDS transmission line, and constitute open termination for reflected waveforms. As a result, signal reflections created by traces, packaging, connectors, and the cable can arrive at the transmitter with increased amplitude.

To reduce these reflections, the HDMI transmitter port has an internal termination option of 150 Ω for single-ended termination, and 300 Ω for differential termination. This termination reduces the amplitude of the reflected signal, but it also lowers the common mode input voltage at the sink. Lattice Semiconductor recommends turning internal source termination off when the transmitter operates less than or equal to 165 MHz, and turning it on for frequencies above 165 MHz.

2.13.4. HDCP Encryption Engine/XOR Mask

The HDMI transmitter provides an HDCP encryption engine that contains the logic necessary to encrypt the incoming audio and video data, and includes support for HDCP authentication and repeater checks. The system microcontroller controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selection Vector (KSV), stored in the HDCP key ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle.

2.13.5. HDCP Key ROM

The SiI9612 video processor comes preprogrammed with a set of production HDCP keys for the HDMI transmitter. The keys are stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security because there is no way to read the keys once the device is programmed.

Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Lattice Semiconductor before receiving SiI9612 samples.

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2.13.6. Audio Return Channel

The SiI9612 video processor provides an Audio Return Channel (ARC) input to receive an IEC60958-1 or IEC61937 audio stream from the connected sink device through the utility pin of the HDMI cable.

The SiI9612 device supports only single mode ARC. The SiI9612 ARC input can be made compatible for common mode ARC by using an AC-coupling network between the HPD and utility pins of the HDMI connector of the HDMI output port and the SiI9612 ARC pin.

2.13.7. DDC Master I²C Interface

The SiI9612 HDMI transmitter includes a DDC master I²C interface for direct connection to the HDMI cable. The DDC master I²C interface is used for two purposes:

- To read the EDID of the connected downstream device,
- To perform HDCP authentication of the connected downstream device.

The host uses the DDC master logic to read the EDID by programming the target address, offset, and number of bytes. When completed, or when the DDC master FIFO becomes full, an interrupt signal is sent to the host so that the host can read data out of the FIFO.

The TPI hardware uses the DDC master to carry out HDCP authentication tasks. The request to perform HDCP authentication is initiated by the host, but it does not access the DDC master directly.

2.13.8. Receiver Sense and Hot Plug Detection

The HDMI transmitter can detect a connected device through the Hot Plug Detect (HPD) input signal or the internal Receiver Sense (RSEN) logic. When HIGH, the HPD signal indicates to the transmitter that the EDID of the connected receiver is readable. The RSEN can be used to detect whether the attached device is powered by sensing the termination in the attached device. An interrupt can be generated whenever there is a change in the state of the HPD or RSEN signal.

2.13.9. Interrupts

The Interrupt logic in the HDMI transmitter buffers interrupt events from different sources. Receiver Sense and Hot Plug Interrupts are also available in power-down mode. The logic for handling these interrupts when all clocks are disabled is also part of this block. The INT pin provides an interrupt signal to the system microcontroller when any of the following occur:

- Monitor Detect (either from the HPD input level or from the receiver sense feature) changes
- VSYNC (useful for synchronizing a microcontroller to the vertical timing interval)
- Error in the audio format
- DDC FIFO status changes
- HDCP authentication error

2.14.HDMI Input

The SiI9612 video processor integrates an HDMI receiver that accepts 300 MHz inputs such as 1080p @ 60 Hz 3D and 4K x 2K video formats. It offers a full video and audio processing pipeline, integrated HDCP keys, and a decryption engine. MHL mode is available with support for PackedPixel mode.

2.14.1. TMDS Receiver Core

The HDMI receiver core is the latest generation core and can receive TMDS data up to 300 MHz. The core performs 10- to 8-bit TMDS decoding on the video data, and 10- to 4-bit TMDS decoding on the audio data received from the three TMDS differential data lines, along with a TMDS differential clock. The TMDS core can sense a stopped clock or stopped video and software can put the video processor into power down mode.

Adaptive equalization is applied to the input signal to counter high-frequency attenuation resulting from long cables, thus ensuring reliable data recovery.

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The receiver core operates in either HDMI or MHL mode. In MHL mode, the receiver core demultiplexes a single TMDS data channel into its three component logical channels (two for PackedPixel mode) of 8 bits each using a common mode clock signal carried on the same TMDS channel.

2.14.2. Deep Color Support

The SiI9612 video processor detects deep color packets in the HDMI data stream and automatically decodes the proper pixel clock setting and output bus width. The deep color mode can be read from registers as 24 bits, 30 bits, or 36 bits per pixel, up to 1080p @ 60 Hz. An interrupt can be generated whenever the deep color mode changes.

2.14.3. MHL Receiver

The HDMI input of the SiI9612 video processor can be configured as a Mobile High-definition Link (MHL) receiver. When an MHL source is connected, an MHL cable detect sense signal from the cable is asserted and sent to the SiI9612 device, and also to the host microcontroller as an interrupt to configure the receiver port as an MHL port, and to prepare for the CBUS discovery process.

The MHL receiver supports PackedPixel mode, which encodes YCbCr 4:2:2 pixel data using 16 bits per pixel rather than 24 bits per pixel as in the other pixel encoding modes. The incoming pixel clock rate may be as high as 150 MHz in this mode, with a link clock rate of half of the pixel clock, which allows MHL to support 1080p @ 60 Hz video. The maximum link clock rate remains 75 MHz in PackedPixel mode.

2.14.4. HDCP Decryption Engine/XOR Mask

The HDMI receiver provides an HDCP decryption engine to decrypt protected audio and video data transmitted by the source device. Decryption is enabled only after the successful completion of an authentication protocol between the source device and the HDMI receiver. This process is driven by the source device through a set sequence of read and writes through the DDC channel. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio-visual data.

The HDMI receiver also contains all the necessary logic to support full HDCP repeaters. The KSV FIFO can store a KSV list consisting of up to 16 devices.

2.14.5. HDCP Embedded Keys

The SiI9612 device is preprogrammed with a set of production HDCP keys for the HDMI receiver. The keys are stored on the chip in nonvolatile memory. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. Before receiving samples of the SiI9612 video processor, customers must sign the HDCP license agreement (available from Digital Content Protection LLC) or a special NDA with Lattice Semiconductor.

2.14.6. EDID RAM Block

An EDID block is supported on the HDMI receiver port. The EDID block consists of 256 bytes of RAM to contain the EDID data structure. This memory, comprised of SRAM, is volatile and must be initialized by software during power up.

2.15.Audio Input Processing

The SiI9612 video processor provides multiple ways to accept digital audio signals for insertion onto the HDMI output stream. The HDMI transmitter receives the audio stream through an I^2S or S/PDIF port. Audio data can come from one of many sources for each interface, controlled by a multiplexer. This is illustrated in Figure 2.2 on page 9.

All major audio encoding formats are supported, including LPCM audio, one-bit audio, and bitstream audio formats including high-bitrate audio.

2.15.1. I^2S Audio Input

There are two external I^2S ports on the SiI9612 device. The first I^2S port is comprised of three signal pins: AI_SCK, AI_WS, and AI_SD. The signal pins are dedicated inputs intended to support 2-channel linear pulse code modulation (LPCM) audio. This I^2S input port accepts audio sample frequencies of 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz.

The second I^2S port has seven signal pins: AO_MCLK, AO_SCK, AO_WS, and AO_SD[3:0]. All pins except AO_MCLK are bidirectional. The direction of these pins is controlled by a software programmable register. These pins default to

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outputs. When the pins are configured as inputs, they enable an input of up to eight channels of LPCM audio for insertion onto the HDMI output. The I²S input supports sampling frequencies of 32 to 192 kHz.

The multichannel I²S interface also supports high-bitrate audio formats like Dolby® TrueHD and DTS-HD Master Audio™.

Only one of the I²S ports can be selected to send audio data to the HDMI transmitter at any given time.

2.15.2. Direct Stream Digital Input

Seven pins are used for the Direct Stream Digital (DSD) interface that provides 6-channel one-bit audio data. This interface is for Super Audio Compact Disc (SACD) applications. The DSD input pins are mapped to the multichannel I²S pins and the S/PDIF input pin of the SiI9612 device as shown in Table 2.3 below.

The one-bit audio inputs are sampled on the positive edge of the DSD clock, assembled into 56-bit packets, and mapped to the appropriate FIFO. The Audio InfoFrame, instead of the Channel Status bits, carries the sampling information for one-bit audio. The one-bit audio interface supports input clock frequencies of 2.822 MHz (64 • 44.1 kHz) and 5.645 MHz (64 • 88.2 kHz).

Table 2.3. DSD Input Pin Mapping

DSD Signal	Pin #	Pin Name
DCLK	33	AO_SCK
DR0	34	AO_WS
DL0	32	AO_SD0
DR1	31	AO_SD1
DL1	30	AO_SD2
DR2	29	AO_SD3
DL2	28	AI_SPDIF

2.15.3. S/PDIF Input

The SiI9612 device can accept digital audio from a S/PDIF input pin. The Sony/Philips Digital Interface Format (S/PDIF) interface is usually associated with compressed audio formats such as Dolby® Digital (AC-3), DTS, and the more advanced variants of these formats. The S/PDIF interface also supports the LPCM format at sampling frequencies of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz.

2.15.4. Requirement for an MCLK

The video processor includes an integrated MCLK generator for operation without requiring an external clock PLL. This removes the requirement for an MCLK input on the device for creating the time stamp value used in audio clock recovery.

2.15.5. Audio Downsampler

The SiI9612 device has an audio downsampler function that downsamples the incoming two-channel audio data and sends the result over the HDMI link. The audio data can be downsampled by one-half or one-fourth with register control. Conversions from 192 kHz to 48 kHz, 176.4 kHz to 44.1 kHz, 96 kHz to 48 kHz, and 88.2 kHz to 44.1 kHz are supported. Some limitations in the audio sample word length, when using this feature, may need special consideration in a real application.

When enabling the audio downsampler, the Channel Status registers for the audio sample word lengths sent over the HDMI link always indicate the maximum possible length. For example, if the input S/PDIF stream was in 20-bit mode with 16 bits valid after enabling the downsampler, the Channel Status indicates 20-bit mode with 20 bits valid.

Audio sample word length is carried in bits 33 through 35 of the Channel Status register over the HDMI link, as shown in Table 2.4 on the next page. These bits are always set to 0b101 when enabling the downsampler feature. Audio data is not affected because zeroes are placed into the LSBs of the data, and the wider word length is sent across the HDMI link.

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Table 2.4. Channel Status Bits Used for Word Length

Bit				Sample Word Length (bits)	Note
Audio Sample Word Length			Maximum Word Length[1]		
35	34	33	32		
0	0	0	0	Not Indicated	—
0	0	1	0	16	2
0	1	0	0	18	2
1	0	0	0	19	2
1	0	1	0	20	2, 4
1	1	0	0	17	2
0	0	0	1	Not Indicated	3
0	0	1	1	20	3
0	1	0	1	22	3
1	0	0	1	23	3
1	0	1	1	24	3, 4
1	1	0	1	21	3

Notes:

1. Maximum audio sample word length (MAXLEN) is 20 bits if MAXLEN = 0 and 24 bits if MAXLEN = 1.
2. Maximum audio sample word length is 20.
3. Maximum audio sample word length is 24.
4. Bits [35:33] are always 0b101 when the downsampler is enabled.

2.15.6. High-bitrate Audio on HDMI

The high-bitrate compression standards, such as Dolby® TrueHD and DTS-HD Master Audio™, transmit data at bitrates as high as 18 Mb/s or 24 Mb/s. Because these bit rates are so high, Blu-ray decoders, HDMI transmitters (as source devices), and DSPs and HDMI receivers (as sink devices) must carry the data using four I²S lines rather than using a single very-high-speed S/PDIF interface or I²S bus (see Figure 2.7).

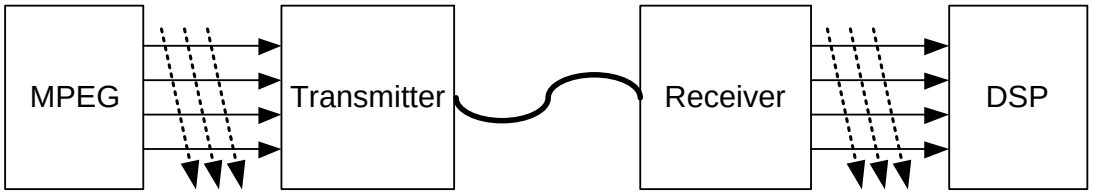

Figure 2.7. High-speed Data Transmission

The high-bitrate audio stream is originally encoded as a single stream. To send the stream over four I²S lines, the DVD decoder splits it into four streams. Figure 2.8 shows the high-bitrate stream before it has been split into four I²S lines, and Figure 2.9 on the next page shows the same audio stream after being split. Each sample requires 16 cycles of the I²S clock (SCK).

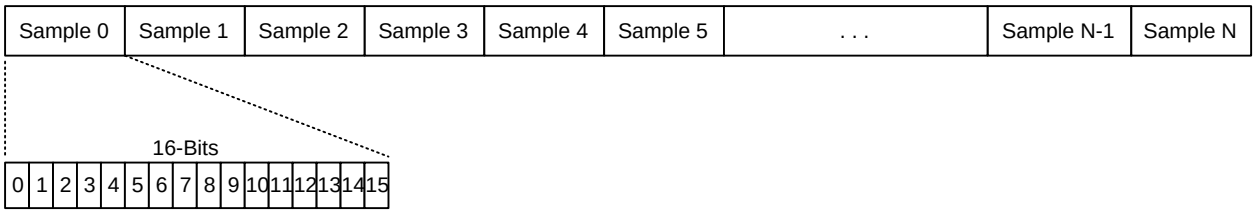

Figure 2.8. High-bitrate Stream before and after Reassembly and Splitting

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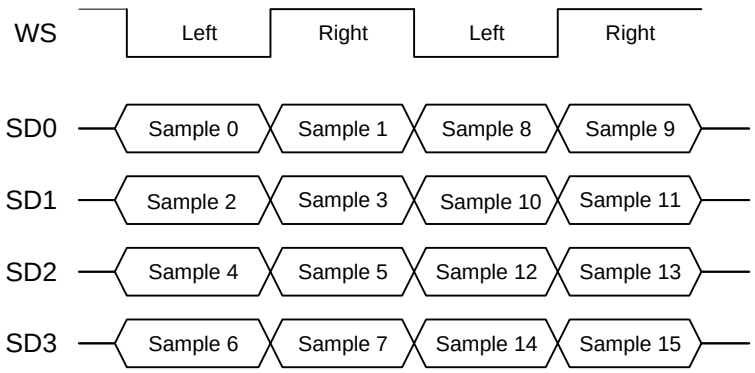

Figure 2.9. High-bitrate Stream after Splitting

2.15.7. I²S-to-SPDIF Conversion

The SiI9612 video processor includes audio processing to convert LPCM audio from the 2-channel I²S input or from the I²S output of the HDMI receiver to an IEC 60958 formatted audio stream. The converted audio stream is sent to the S/PDIF output pin. The conversion works only for 2-channel audio.

2.16.Audio Output Processing

The SiI9612 video processor supports audio extraction from the received HDMI/MHL streams. It can send the digital audio to a S/PDIF output, four I²S outputs (SD[3:0]), or six one-bit audio outputs. In addition, the audio output signals can be routed directly to the audio input ports of the HDMI transmitter using an internal audio data path.

Internal routing, multiplexing and processing of I²S and S/PDIF audio signals are illustrated in Figure 2.2 on page 9.

2.16.1. S/PDIF Output

The S/PDIF output transmits 2-channel uncompressed LPCM data (IEC 60958) or a compressed bitstream for multichannel (IEC 61937) formats. The audio data output logic forms the audio data output stream from the HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 kHz to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time stamping purposes.

2.16.2. I²S Audio Output

An I²S output port with four data lines on the SiI9612 device enables 8-channel digital audio output at sample rates from 32 to 192 kHz. The I²S interface is highly programmable through registers to allow interfacing with a wide range of audio DACs or audio DSPs with I²S inputs. The I²S output port consists of signal pins AO_MCLK, AO_SCK, AO_WS, and AO_SD[3:0].

Additionally, an MCLK output signal is provided with a frequency that is programmable as an integer multiple of the audio sample rate f_S. MCLK frequencies support various audio sample rates as shown in Table 2.5.

Table 2.5. Supported MCLK Frequencies

Multiple of f_S	Audio Sample Rate, f_S: I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	—	—
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—

The I²S output pins can be reconfigured as inputs for source-specific applications, such as a Blu-ray player where the SoC supplies the multichannel audio to the SiI9612 device directly through the I²S bus.

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2.16.3. One-bit Audio Output

The SiI9612 device can output six DSD/SACD streams and a clock for up to 6-channel support. The DSD streams are output on the multichannel I²S pins and the S/PDIF output pin according to Table 2.6. One-bit audio supports 64 • f_S, with f_S being 44.1 kHz or 88.2 kHz.

The one-bit audio outputs are synchronous to the positive edge of the DSD Clock. For one-bit audio, the sampling information is carried in the Audio InfoFrame instead of the Channel Status bits.

Table 2.6. DSD Output Pin Mapping

DSD Signal	Pin #	Pin Name
DCLK	33	AO_SCK
DR0	34	AO_WS
DL0	32	AO_SD0
DR1	31	AO_SD1
DL1	30	AO_SD2
DR2	29	AO_SD3
DL2	37	AO_SPDIF

2.16.4. High-bitrate Audio Support

The SiI9612 video processor supports the extraction of high-bitrate audio packets from the HDMI input. The extracted data is streamed out through the I²S output port on four I²S data lines at 192 kHz packet rate each.

Figure 2.10 shows the layout of the high-bitrate audio samples on the four I²S lines.

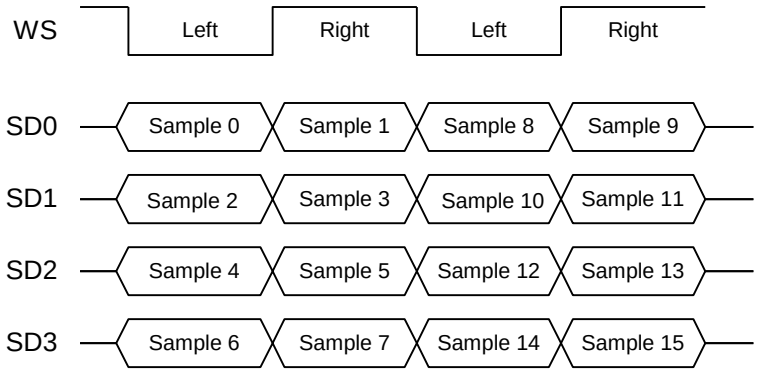

Figure 2.10. Layout of High-bitrate Audio Samples on I²S

2.16.5. Auto Audio Configuration

The SiI9612 video processor can control the audio output based on the current states of CablePlug, FIFO, Video, ECC, ACR, PLL, InfoFrame and HDMI. Audio output is only enabled when all necessary conditions are met. If any critical condition is missing, the audio output is disabled automatically. Each of these events, which the logic monitors, can be turned on or off separately through a set of programmable registers.

2.16.6. Soft Mute

On command from a register bit or when automatically triggered with Automatic Audio Control (AAC), the video processor progressively reduces the audio data amplitude to mute the sound in a controlled manner. This is useful when there is an interruption to the HDMI audio stream (or an error) to prevent any audio pop from being sent to the I²S or S/PDIF outputs.

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2.17.CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. A CEC controller compatible with the Lattice Semiconductor CEC Programming Interface (CPI) is included on the chip. This CEC controller has a high-level register interface accessible through the I^2C or SPI interface and can send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus.

2.18.GPIO

The SiI9612 video processor has four General Purpose I/O (GPIO) pins. Each GPIO pin supports the following functions:

- Input mode: The value can be read through a register.
- Output mode: The value can be set through a programmable register.

The GPIO pins can be reconfigured as a Serial Peripheral Interface (SPI) interface for programming the chip. Refer to the Pin Strapping section on page 25 for more information.

2.19.Control and Configuration

2.19.1. Register/Configuration Logic

The register/configuration logic block incorporates all the registers required for configuring and managing the features of the SiI9612 video processor. These registers are used to perform HDCP authentication, audio/video/auxiliary format processing, CEA-861B InfoFrame packet format, and power-down control.

The registers are accessible from one of two I^2C serial ports. The first is the DDC port located on the HDMI receiver port, and is connected through the HDMI cable to the upstream HDMI transmitter. It is used to exchange values between the transmitter and the SiI9612 video processor for HDCP operation. The second is the local I^2C port that controls the SiI9612 device from the display system. The local device registers controlled by the display system can also be accessed through a Serial Peripheral Interface (SPI) bus.

The local device registers are accessed using a 16-bit addressing scheme. Refer to the Feature Information section on page 44 for details.

2.19.2. I^2C Serial Ports

The SiI9612 video processor provides three I^2C serial interfaces:

- DDC receiver port to communicate back to the upstream HDMI or DVI host,
- DDC master port to read the EDID or perform HDCP authentication of the downstream device,
- I^2C port for initialization and control by a local microcontroller in the display.

Refer to the Feature Information section on page 44 for a more detailed description of these serial ports.

The device address for the local I^2C interface can be set as 0x30 or 0x32 through a strapping pin (see Table 2.7).

2.19.3. SPI Serial Bus

The SiI9612 device SPI serial interface employs a simple four-wire synchronous serial interface with unidirectional data lines. The SPI interface allows the local microcontroller to access the SiI9612 device registers at up to 10 MHz bitrate. This is a more efficient method of configuring the device when compared to I^2C mode.

Refer to the Feature Information section on page 44 for a more detailed description of SPI.

2.19.4. Delay from Reset Deactivation to Register Access

Once the Reset pin of the SiI9612 device is deactivated, the software must wait 100 ns before accessing the device registers through either the local I^2C or SPI bus.

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2.20.Pin Strapping

The SiI9612 device supports pin strapping configuration to select the default device I^2C address and the mode of the SPI pins. These settings are shown in Table 2.7. The logical value on these pins is latched by the SiI9612 device on the rising edge of RESET. See the

Digital Audio Output Pins table on page 40 for more information.

Table 2.7. Pin Strapping Options

Pin Name	Mode Name	Description
AO_MUTE	I2C_ADDRSEL	Select I^2C Address (0x30/0x32). 0 – Address 0x30 1 – Address 0x32
AO_SPDIF/DL2(OUT)	GPIO_MODE	Select GPIO Mode. 0 – SPI pins used as SPI 1 – SPI pins used as GPIO

2.21.Power Supply Sequencing

There are no power supply sequencing requirements for the SiI9612 device.

2.22.Audio PLL Reset

Once the SiI9612 device is powered on and all the power supplies of the device have reached their normal operating voltages, the audio PLL must be reset to ensure normal operation. The audio PLL is reset by asserting its Power Down bit for at least 1 ms.

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3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
IO_VDD33	I/O Pin Supply Voltage	–0.3	—	4.0	V	1, 2, 3
IO_APVDD33	Audio PLL I/O Supply Voltage	–0.3	—	4.0	V	1, 2, 3
RX_AVDD10	TMDS RX Analog 1.0 V Supply Voltage	–0.3	—	1.5	V	1, 2
RX_AVDD33	TMDS RX Analog 3.3 V Supply Voltage	–0.3	—	4.0	V	1, 2
TX_AVDD10	TMDS TX Analog Supply Voltage	–0.3	—	1.5	V	1, 2
TX_PVDD10	TMDS TX PLL Supply Voltage	–0.3	—	1.5	V	1, 2
VP_AVDD10	Video PLL Supply Voltage	–0.3	—	1.5	V	1, 2
AP_AVDD10	Audio PLL Supply Voltage	–0.3	—	1.5	V	1, 2
DVDD10	Digital Logic Supply Voltage	–0.3	—	1.5	V	1, 2
IO_VDD5	I/O Pin 5 V Supply Voltage	–0.3	—	5.7	V	1, 2
V_I	Input Voltage	–0.3	—	IO_VDD33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V tolerant Pins	–0.3	—	5.7	V	—
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under normal operating conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to the SiI9612 Qualification Report for information on ESD performance.

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
IO_VDD33	I/O Pin Supply Voltage	3.14	3.3	3.47	V	—
IO_APVDD33	Audio PLL I/O Supply Voltage	3.14	3.3	3.47	V	—
RX_AVDD10	TMDS RX Analog 1.0 V Supply Voltage	0.95	1.0	1.05	V	—
RX_AVDD33	TMDS RX Analog 3.3 V Supply Voltage	3.14	3.3	3.47	V	—
TX_AVDD10	TMDS TX Analog Supply Voltage	0.95	1.0	1.05	V	—
TX_PVDD10	TMDS TX PLL Supply Voltage	0.95	1.0	1.05	V	—
VP_AVDD10	Video PLL Supply Voltage	0.95	1.0	1.05	V	—
AP_AVDD10	Audio PLL Supply Voltage	0.95	1.0	1.05	V	—
DVDD10	Digital Logic Supply Voltage	0.95	1.0	1.05	V	—
IO_VDD5	I/O Pin 5 V Supply Voltage	4.75	5.0	5.25	V	1
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	25	°C/W	2

Notes:
1. The IO_VDD5 pin is the supply voltage for the CSCL, CSDA, CEC, CDSENSE, TX_DSCL, TX_DSDA, RX_DSDA, RX_DSCL and RX_HPD/CBUS pins. It must be connected to a 5 V power supply.
2. Airflow at 0 m/s. 4-layer PCB.

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3.3. DC Specifications

Table 3.3. Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH-level Input Voltage	LVTTL Schmitt	—	2.0	—	—	V	—
V_{IL}	LOW-level Input Voltage	LVTTL Schmitt	—	—	—	0.8	V	—
DDC V_{TH+}	LOW-to-HIGH Threshold, DDC Bus	Schmitt	—	3.0	—	—	V	2
DDC V_{TH-}	HIGH-to-LOW Threshold, DDC Bus	Schmitt	—	—	—	1.5	V	2
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V	—
V_{OL}	LOW-level Output Voltage	LVTTL	—	—	—	0.4	V	—
$V_{OL\ DDC}$	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
$V_{OL\ I2C}$	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
I_{OL}	Output Leakage Current	—	High-impedance	–10	—	100	µA	3
I_{IL}	Input Leakage Current	—	High-impedance	–10	—	100	µA	4
I_{OD6}	6 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	6	—	—	mA	—
			V_{OUT} = 0.4 V	6	—	—	mA	—
I_{OD8}	8 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	8	—	—	mA	—
			V_{OUT} = 0.4 V	8	—	—	mA	—
R_{PD}	Internal Pull-down Resistor	Outputs	—	—	46	—	kΩ	—
I_{OPD}	Output Pull-down Current	Outputs	IO_VDD33 = 3.47 V	—	—	100	µA	3
I_{IPD}	Input Pull-down Current	Input	IO_VDD33 = 3.47 V	—	—	100	µA	4

Notes:

1. Refer to the Pin Diagram and Pin Descriptions section beginning on page 38 for pin type designations for all package pins.
2. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
3. The chip includes an internal pull-down resistor on many of the output pins. When in the high-impedance state, these pins draw a pull down current according to this specification when the signal is driven HIGH by another source device.
4. The chip includes an internal pull-down resistor on many of the input pins. These pins draw a pull-down current according to these values when the signal is driven HIGH by another device.

Table 3.4. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDFH}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICMH}	Common Mode Input Voltage	—	RX_AVDD33 – 400	—	RX_AVDD33 – 37.5	mV

Table 3.5. TMDS Input DC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	RX_AVDD33 – 1200	—	RX_AVDD33 – 300	mV
V_{IDFM}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICMM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

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Table 3.6. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SWING}	Single-ended Output Swing Voltage	RLOAD = 50 Ω	400	—	600	mV
V_H	Single-ended HIGH-level Output Voltage	≤ 165 MHz TMDS clock	TX_AVDD33 – 10	—	TX_AVDD33 + 10	mV
		> 165 MHz TMDS clock	TX_AVDD33 – 200	—	TX_AVDD33 + 10	mV
V_L	Single-ended LOW-level Output Voltage	≤ 165 MHz TMDS clock	AVDD33 – 600	—	AVDD33 – 400	mV
		> 165 MHz TMDS clock	AVDD33 – 700	—	AVDD33 – 400	mV

Table 3.7. Single Mode Audio Return Channel DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IS_ARC}	Input Swing Amplitude	—	160	—	600	mV

Table 3.8. CEC DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH+CEC}	LOW-to-HIGH Threshold	—	2.0	—	—	V
V_{TH-CEC}	HIGH-to-LOW Threshold	—	—	—	0.8	V
V_{OH_CEC}	HIGH-level Output Voltage	—	2.5	—	—	V
V_{OL_CEC}	LOW-level Output Voltage	—	—	—	0.6	V
I_{IL_CEC}	Input Leakage Current	Power Off	—	—	1.8	µA

Table 3.9. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	High-level Input Voltage	—	1.0	—	—	V
V_{IL_CBUS}	Low-level Input Voltage	—	—	—	0.6	V
V_{OH_CBUS}	High-level Output Voltage	I_{OH} = 100 µA	1.5	—	1.9	V
V_{OL_CBUS}	Low-level Output Voltage	I_{OL} = –100 µA	—	—	0.2	V
Z_{DSC_CBUS}	Pull-down Resistance – Discovery	—	800	1000	1200	Ω
Z_{ON_CBUS}	Pull-down Resistance – Active	—	90	100	110	kΩ
I_{IL_CBUS}	Input Leakage Current	High-impedance	—	—	1	µA
C_{CBUS}	Capacitance	Power On	—	—	80	pF

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3.3.1. DC Power Supply Pin Specifications

Table 3.10. Total Power Dissipation

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IO_VDD33}	Supply Current for IO_VDD33	—	—	—	6	mA
$I_{IO\_APVDD33}$	Supply Current for IO_APVDD33	—	—	—	5	mA
I_{RX_AVDD10}	Supply Current for RX_AVDD10	—	—	—	56	mA
I_{RX_AVDD33}	Supply Current for RX_AVDD33	—	—	—	61	mA
I_{TX_AVDD10}	Supply Current for TX_AVDD10	—	—	—	34	mA
I_{TX_PVDD10}	Supply Current for TX_PVDD10	—	—	—	8	mA
I_{VP_AVDD10}	Supply Current for VP_AVDD10	—	—	—	12	mA
I_{AP_AVDD10}	Supply Current for AP_AVDD10	—	—	—	3	mA
I_{DVDD10}	Supply Current for DVDD10	—	—	—	784	mA
I_{IO_VDD5}	Supply Current for IO_VDD5	—	—	—	7	mA
Total	Total Power	—	—	—	1.23	W

Notes: Maximum power dissipation has been measured under the following operating conditions:

1. 70 °C ambient temperature with device power supplies set to 5% over normal operating values.
2. Scaling 480p @ 60 Hz to 1080p @ 60 Hz with a pseudo random test pattern and video processing enabled.

Table 3.11. Power-down Mode Power Dissipation

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{PD_1V}	1 V Power Supply Current	—	—	—	220	mA
$I_{PD\_3.3V}$	3.3 V Power Supply Current	—	—	—	7	mA
I_{PD_5V}	5 V Power Supply Current	—	—	—	7	mA
Total	Total Power	—	—	—	292	mW

Note: Maximum power dissipation has been measured at 70 °C ambient temperature with supplies set to 5% over normal operating values, and no switching applied on the input and output ports.

3.4. AC Specifications

Table 3.12. TMDS Input AC Timing Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{DPS}	Intrapair Differential Input Skew	@300 MHz	—	—	$0.15T_{BIT} + 112$	ps	—
T_{CCS}	Channel-to-Channel Differential Input Skew	—	—	—	$0.2T_{PIXEL} + 1.78$	ns	Figure 4.3
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz	—
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns	—
T_{DIJIT}	Differential Input Clock Jitter Tolerance	@300 MHz	—	—	0.3	T_{BIT}	—

Table 3.13. TMDS Input AC Timing Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intrapair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common Mode Intrapair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns
T_{CLOCK_JIT}	Common Mode Clock Jitter Tolerance	@300 MHz	—	—	$0.8T_{BIT}$	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	@300 MHz	—	—	$0.6T_{BIT}$	Ps

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Table 3.14. TMDS Output AC Timing Specifications Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intrapair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	20% – 80%	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	80% – 20%	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DCDUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}
T_{DOJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

Table 3.15. CEC AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{R_CEC}	Rise Time	10% – 90%	—	—	250	µs
T_{F_CEC}	Fall Time	90% – 10%	—	—	50	µs

Table 3.16. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{BIT_CBUS}	Bit Time	1 MHz clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V – 1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V – 1.5 V	5	—	200	ns
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns

Table 3.17. I²S Audio Input Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I²S Cycle Time	—	—	—	1.0	UI	Figure 4.4	1
$T_{SCKIDUTY}$	I²S Duty Cycle	—	90%	—	110%	UI	Figure 4.4	1
T_{I2SSU}	I²S Setup Time	—	15	—	—	ns	Figure 4.4	2
T_{I2SHD}	I²S Hold Time	—	5	—	—	ns	Figure 4.4	2

Notes:

1. Proportional to unit time (UI) according to sample rate. Refer to the I²S Specification.
2. Set up and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I²S Specification.
3. All parameters are applicable to the I²S output port signals when reconfigured as inputs.

Table 3.18. S/PDIF Input Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_SPDIF}	Sample Rate	—	32	—	192	kHz	—
T_{SPICYC}	AI_SPDIF Cycle Time*	—	—	—	1.0	UI	Figure 4.5
$T_{SPIDUTY}$	AI_SPDIF Duty Cycle*	—	90%	—	110%	UI	Figure 4.5

***Note:** Proportional to unit time (UI) according to sample rate. Refer to the IEC60958 Specification.

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Table 3.19. I²S Audio Output Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{TR}	AO_SCK Clock Period	C_L = 10 pF	1.00	—	—	T_{tr}	Figure 4.6	1, 2
T_{HC}	AO_SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{tr}		1, 2
T_{LC}	AO_SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{tr}		1, 2
T_{SU}	Setup Time, AO_SCK to AO_SD/WS	C_L = 10 pF	$0.4T_{tr} - 5$	—	—	ns		1, 2
T_{HD}	Hold Time, AO_SCK to AO_SD/WS	C_L = 10 pF	$0.4T_{tr} - 5$	—	—	ns		1, 2
$T_{SCKODUTY}$	AO_SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{tr}		1, 2
T_{SCK2SD}	AO_SCK to AO_SD or AO_WS Delay	C_L = 10 pF	–5	—	+5	ns		1, 3

Notes:
1. Guaranteed by design.
2. Refer to Figure 4.6 on page 35. Meets timings in the Philips I²S Specification.
3. Applies also to SDC-to-WS delay.

Table 3.20. S/PDIF Output Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPOCYC}	AO_SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 4.7	1, 2
F_{SPDIF}	AO_SPDIF Frequency	—	4	—	24	MHz		3
$T_{SPODUTY}$	AO_SPDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2
$T_{MCLKCYC}$	AO_MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 4.8	1
F_{MCLK}	AO_MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1
$T_{MCLKDUTY}$	AO_MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$		—

Notes:
1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. S/PDIF is not a true clock, but is generated from the internal 128 f_S clock, for f_S from 32 to 192 kHz.

Table 3.21. Crystal Clock Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{XTAL}*	External Crystal Freq.	—	26	27	28.5	MHz	Figure 3.1

***Note:** The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

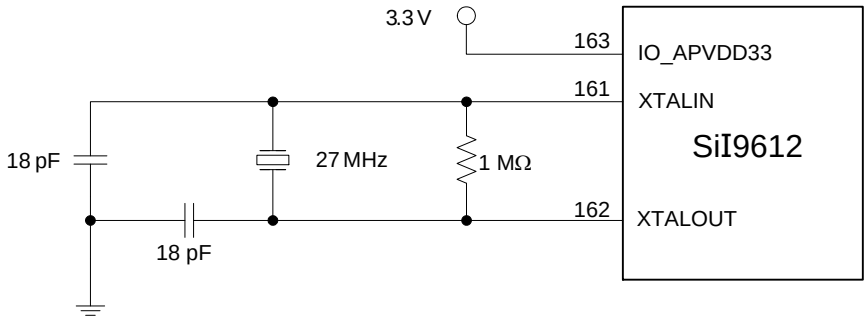

Figure 3.1. Crystal Clock Schematic

3.5. Control Timing Specifications

Table 3.22. Reset Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{RESET}	RESET# Signal LOW Time for Valid Reset	—	10	—	—	µs	Figure 4.1, Figure 4.2

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Table 3.23. I²C Control Signal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid Delay from SCL Falling Edge	C_L = 400 pF	—	—	700	ns	Figure 4.9	—
F_{RXDDC}	Clock Rate on Rx DDC Port	C_L = 400 pF	—	—	100	kHz	—	1
F_{TXDDC}	Clock Rate on Tx DDC Port	C_L = 400 pF	—	—	100	kHz	—	1, 2
F_{I2C}	Clock Rate on Local I²C Port	C_L = 400 pF	—	—	400	kHz	—	3

Notes:

1. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I²C standard mode timings.
2. The operating frequency of the HDMI transmitter DDC port is programmable.
3. Local I²C port (CSCL/CSDA) meets standard mode I²C timing requirements to 400 kHz.

Table 3.24. SPI Control Signal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
tCSs	SPI_CS# Setup Time to SPI_CLK	—	6	—	—	ns	Figure 4.10, Figure 4.11
tCSh	SPI_CS# Hold Time to SPI_CLK	—	6	—	—	ns	Figure 4.10, Figure 4.11
tTXs	SPI_TX Setup Time to SPI_CLK	—	6	—	—	ns	Figure 4.10, Figure 4.11
tTXh	SPI_TX Hold Time to SPI_CLK	—	6	—	—	ns	Figure 4.10, Figure 4.11
tRXp	SPI_RX Output Time from SPI_CLK Falling Edge	—	1	—	7	ns	Figure 4.11

Note: Signal names are from the perspective of the host.

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4. Timing Diagrams

4.1. Reset Timing Diagrams

VCC must be stable between the limits shown in the Normal Operating Conditions section on page 26 for T_{RESET} before RESET# goes HIGH, as shown in Figure 4.1. Before accessing registers, RESET# must be pulled LOW for T_{RESET}. This can be done by holding RESET# LOW until T_{RESET} after stable power, or by pulling RESET# LOW from a HIGH state for at least T_{RESET}, as shown in Figure 4.2.

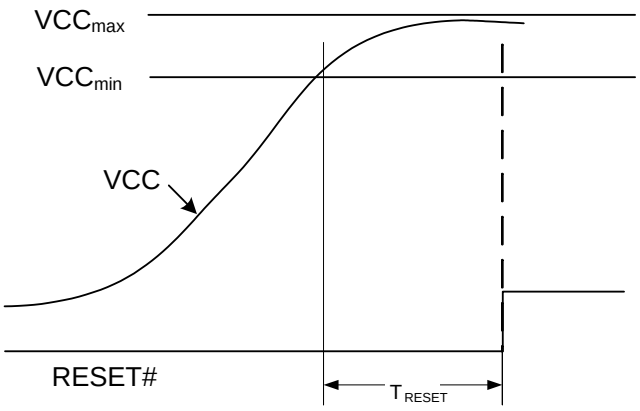

Figure 4.1. Conditions for Use of RESET#

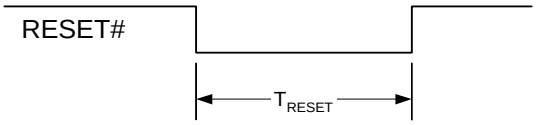

Figure 4.2. RESET# Minimum Timing

4.2. TMDS Input Timing Diagrams

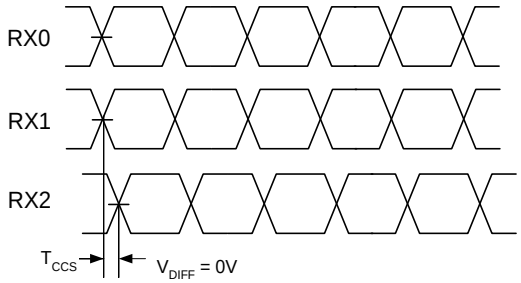

Figure 4.3. TMDS Channel-to-Channel Skew Timing

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4.3. Digital Audio Input Timing Diagrams

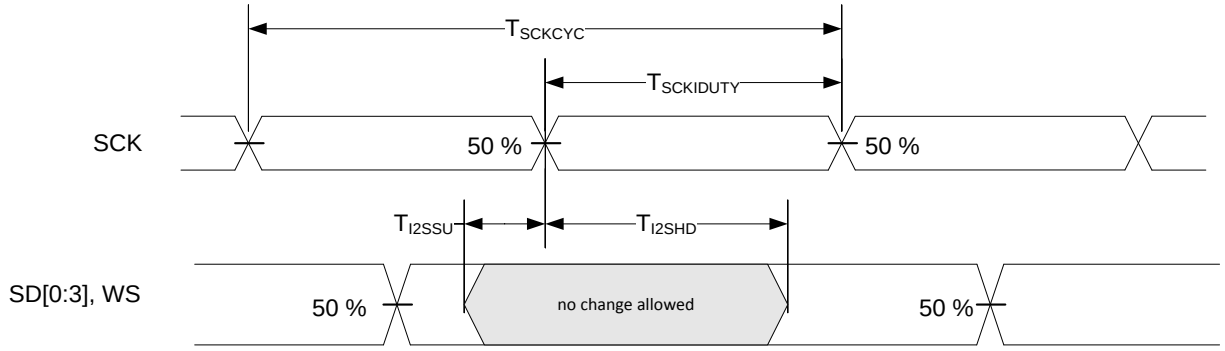

Figure 4.4. I²S Input Timings

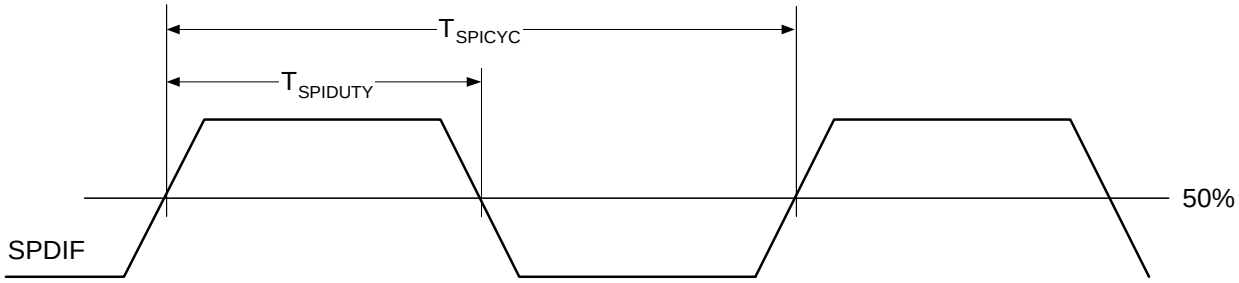

Figure 4.5. S/PDIF Input Timings

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4.4. Digital Audio Output Timing Diagrams

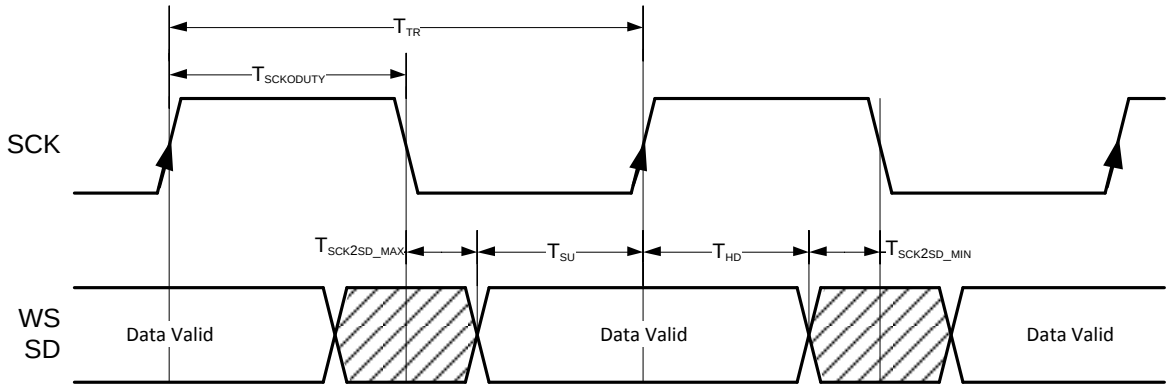

Figure 4.6. I²S Output Timings

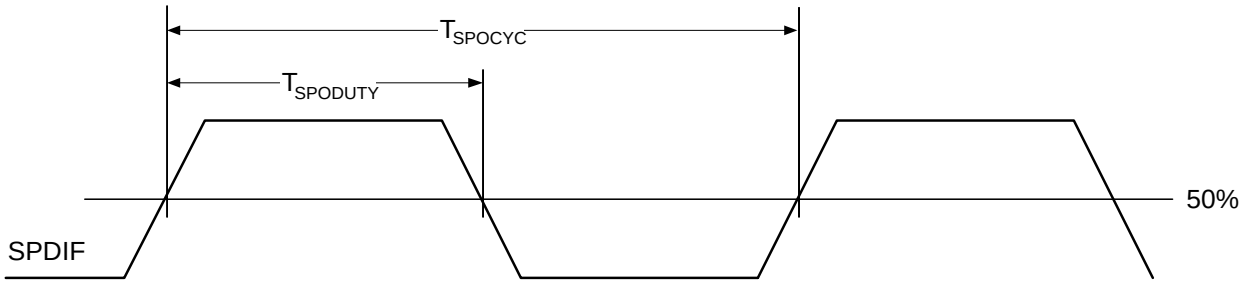

Figure 4.7. S/PDIF Output Timings

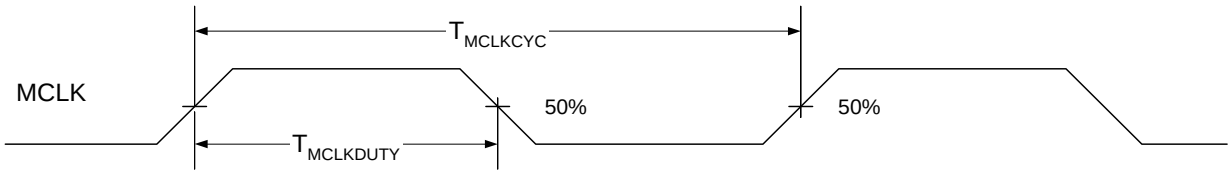

Figure 4.8. MCLK Timings

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4.5. Control Signal Timing Diagrams

4.5.1. I²C Timing Diagram

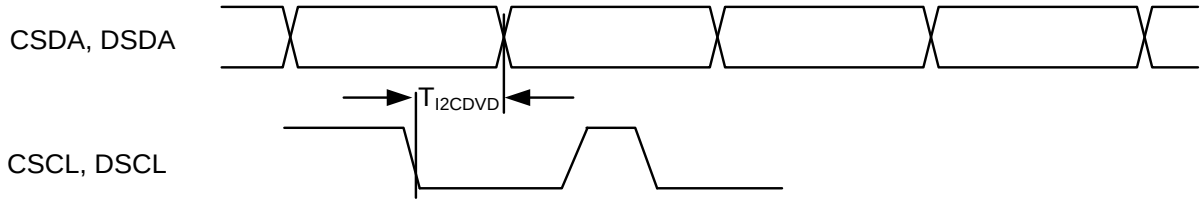

Figure 4.9. I²C Data Valid Delay

4.5.2. SPI Timing Diagrams

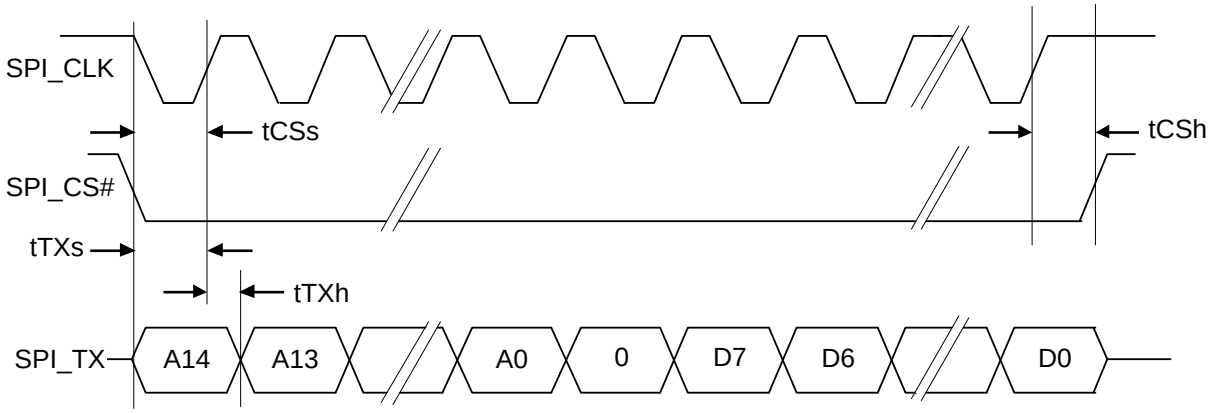

Figure 4.10. SPI Write Setup and Hold Times

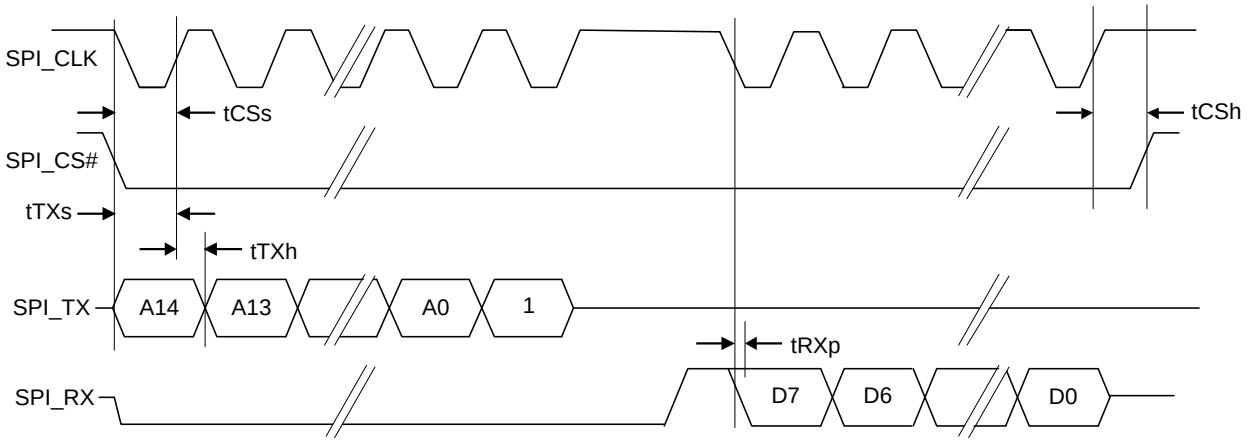

Figure 4.11. SPI Read Setup and Hold Times

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4.6. Calculating Setup and Hold Times for I²S Audio Output Bus

Valid serial data is available at T_{SCK2SD} after the falling edge of the first AO_SCK cycle, and then captured downstream using the active rising edge of AO_SCK one clock period later. The setup time of data-to-AO_SCK (T_{SU}) and hold time of AO_SCK-to-data (T_{HD}) are a function of the worst case AO_SCK-to-output data delay (T_{SCK2SD}). Figure 4.6 on page 35 illustrates this timing relationship. Note that the active AO_SCK edge (rising edge) is shown with an arrowhead. For a falling edge sampling clock, the logic is reversed.

Table 4.1 shows the setup and hold time calculation examples for various audio sample frequencies. The setup and hold times for other audio sampling frequencies can also be calculated with the formula used in these examples.

Table 4.1. I²S Setup and Hold Time Calculations

Symbol	Parameter	FWS (kHz)	FSCK (MHz)	T_{TR} (ns)	Min (ns)
T_{SU}	Setup Time, SCK to SD/WS $= T_{TR} - (T_{SCKDUTY\_WORST} + T_{SCK2SD\_MAX})$ $= T_{TR} - (0.6T_{TR} + 5 ns)$ $= 0.4T_{TR} - 5 ns$	32	2.048	488	190
		44.1	2.822	354	136
		48	3.072	326	125
		96	6.144	163	60
		192	12.288	81	27
T_{HD}	Hold Time, SCK to SD/WS $= (T_{SCKDUTY\_WORST} - T_{SCK2SD\_MIN})$ $= 0.4T_{TR} - 5 ns$	32	2.048	488	190
		44.1	2.822	354	136
		48	3.072	326	125
		96	6.144	163	60
		192	12.288	81	27

Note: The sample calculations shown are based on WS = 64 SCK rising edges.

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5. Pin Diagram and Pin Descriptions

5.1. Pin Diagram

Figure 5.1 shows the pin assignments of the SiI9612 video processor. Individual pin functions are described in the Pin Descriptions section on page 38. The package is a 9 mm × 9 mm, 76-pin MQFN, 0.4 mm pitch, with ePad that must be connected to ground.

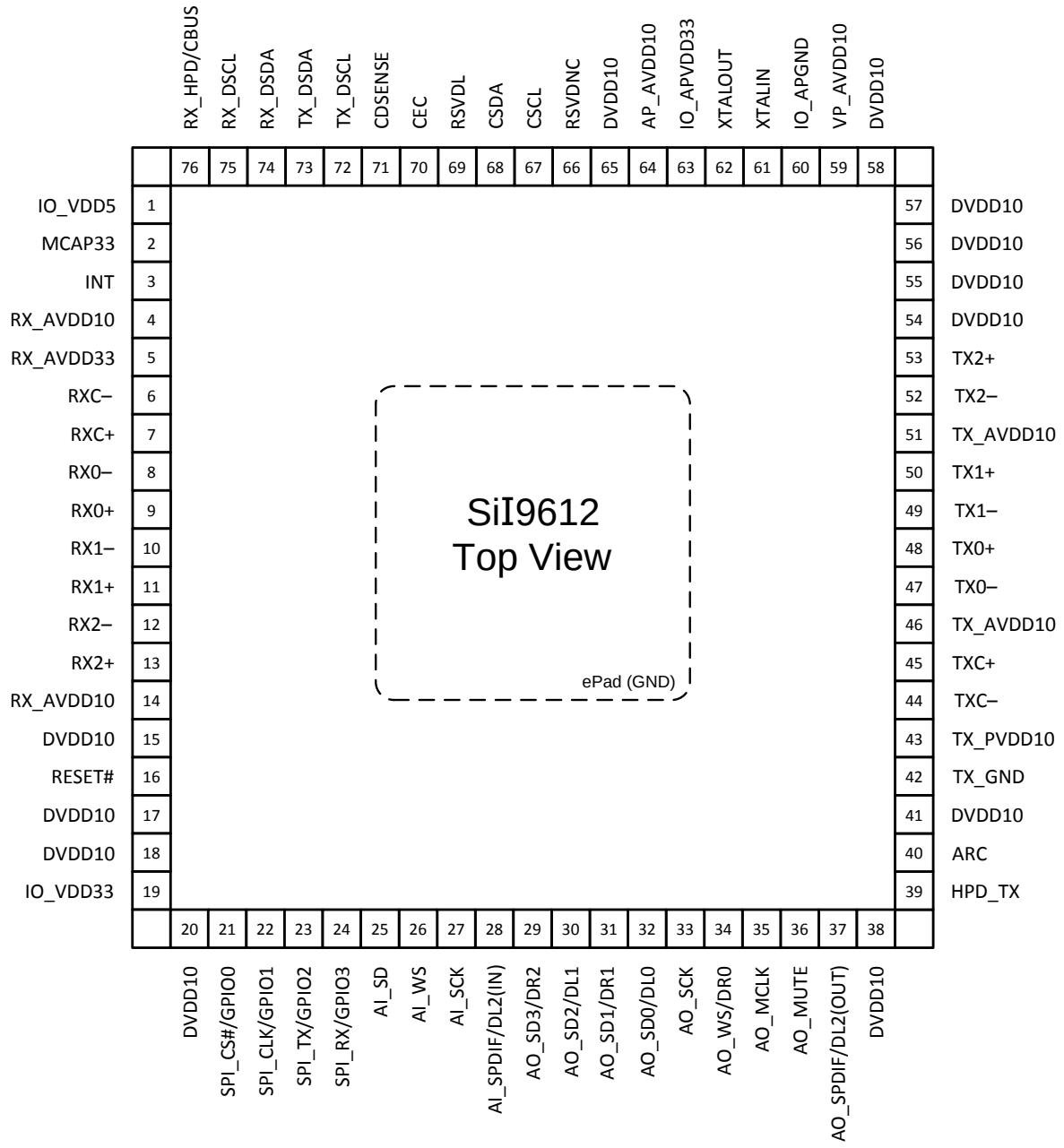

Figure 5.1. Pin Diagram

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5.2. Pin Descriptions

5.2.1. HDMI Receiver Control Signal Pins

Pin Name	Pin	Type	Dir	Description
RX_DSCL	75	Schmitt Open-drain 5 V tolerant	Input	DDC I^2C Clock for HDMI Receiver Port. HDCP KSV, An, and Ri values are exchanged over an I^2C port during authentication. This pin does not present a current path to GND when the device is not powered. This pin requires an external 47 kΩ pull-up resistor as defined in the HDMI Specification.
RX_DSDA	74	Schmitt Open-drain 5 V tolerant	Input Output	DDC I^2C Data for HDMI Receiver Port. HDCP KSV, An, and Ri values are exchanged over an I^2C port during authentication. This pin does not present a current path to GND when the device is not powered.
RX_HPD/CBUS	76	LVTTL/ CBUS 5 V tolerant	Input Output	Hotplug Output Signal to HDMI Connector. In HDMI mode, this is a 5 V signal with 1 kΩ output impedance. It indicates that EDID is readable. In MHL mode, this pin serves as the CBUS signal.
CEC	70	CEC compliant 5 V tolerant	Input Output	HDMI Compliant CEC I/O used to interface to CEC Devices. This pin connects to the CEC signal of all HDMI connectors in the system. This pin has an internal pull-up resistor.
CDSENSE	71	LVTTL Schmitt 5 V tolerant	Input	MHL Cable Detect Sense.

5.2.2. HDMI Receiver Differential Signal Data Pins

Pin Name	Pin	Type	Dir	Description
RX0+	9	TMDS Analog	Input	HDMI Port TMDS Input Data Pairs.
RX0–	8			
RX1+	11			
RX1–	10			
RX2+	13			
RX2–	12			
RXC+	7	TMDS Analog	Input	HDMI Port TMDS Input Clock Pair.
RXC–	6			

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5.2.3. Digital Audio Output Pins

Pin Name	Pin	Type	Dir	Description
AO_MCLK	35	LVTTL 5 V tolerant 6 mA	Output	Audio Master Clock Output. This pin has a weak internal pull-down resistor.
AO_SCK*	33	LVTTL Schmitt 5 V tolerant 6 mA	Output Input	I²S Serial Clock Output or DSD Clock Output. This pin has a weak internal pull-down resistor.
AO_SD3/DR2*	29	LVTTL Schmitt 5 V tolerant 6 mA	Output Input	I²S Serial Ch3 Data Output/DSD Serial Right Ch2 Data Output.
AO_SD2/DL1*	30			I²S Serial Ch2 Data Output/DSD Serial Left Ch1 Data Output.
AO_SD1/DR1*	31			I²S Serial Ch1 Data Output/DSD Serial Right Ch1 Data Output.
AO_SD0/DL0*	32			I²S Serial Ch0 Data Output/DSD Serial Left Ch0 Data Output. AO_SD[3:0] pins have a weak internal pull-down resistor.
AO_WS/ DR0*	34	LVTTL Schmitt 5 V tolerant 6 mA	Output Input	I²S Word Select Output/DSD Serial Right Ch0 Data Output. This pin has a weak internal pull-down resistor.
AO_SPDIF/ DL2(OUT)	37	LVTTL Schmitt 5 V tolerant 6 mA	Input	SPI/GPIO Mode Strapping. This pin is an input when the RESET# pin is asserted. On the rising edge of RESET#, the level on this pin is latched and sets the operational mode of the SPI/GPIO pins. LOW – SPI/GPIO pins are used as SPI signals. HIGH – SPI/GPIO pins are used as GPIO signals. This pin has a weak internal pull-down resistor.
			Output	S/PDIF audio output when the device is not in reset.
				DSD Serial Left Channel 2 data output when device is not in reset.
AO_MUTE	36	LVTTL Schmitt 5 V tolerant 6 mA	Input	Local I²C Slave Address Strapping. This pin is an input when the RESET# pin is asserted. On the rising edge of RESET#, the level on this pin is latched and used to set the address of the local I²C interface. LOW – Address 0x30 HIGH – Address 0x32 This pin has a weak internal pull-down resistor.
			Output	Mute Audio Output. This pin becomes the audio mute output when RESET# is inactive. It is used as a signal to the external downstream audio device, audio DAC, etc. to mute audio output.

***Note**: These I²S audio output signals can be reconfigured by software as inputs to support multichannel audio input.

5.2.4. HDMI Transmitter TMDS Output Pins

Pin Name	Pin	Type	Dir	Description
TX0+	48	TMDS Analog	Output	HDMI Transmitter Output Port Data. TMDS LOW voltage differential signal output data pairs.
TX0–	47			
TX1+	50			
TX1–	49			
TX2+	53			
TX2–	52			
TXC+	45	TMDS Analog	Output	HDMI Transmitter Output Port Clock. TMDS LOW voltage differential signal output clock pair.
TXC–	44			

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5.2.5. HDMI Transmitter Control Signal Pins

Pin Name	Pin	Type	Dir	Description
HPD_TX	39	LVTTL Schmitt 5 V tolerant	Input	Hot Plug Detect. This pin has a weak internal pull-down resistor.
TX_DSCL	72	Schmitt Open-drain 5 V tolerant	Input Output	DDC I^2C Clock for HDMI Transmitter Port. HDCP KSV, An, and Ri values are exchanged over this I^2C port during authentication. This is a true open-drain, so it does not pull to GND if power is not applied. This pin requires an external pull-up resistor between 1.5 to 2.0 kΩ as defined in the HDMI Specification.
TX_DSDA	73	Schmitt Open-drain 5 V tolerant	Input Output	DDC I^2C Data for HDMI Transmitter Port. HDCP KSV, An, and Ri values are exchanged over this I^2C port during authentication. This is a true open-drain, so it does not pull to GND if power is not applied. This pin requires an external pull-up resistor between 1.5 to 2.0 kΩ as defined in the HDMI Specification.

5.2.6. Audio Input Pins

Pin Name	Pin	Type	Dir	Description
AI_SCK	27	LVTTL Schmitt 5 V tolerant	Input	I^2S Serial Clock Input. This pin has a weak internal pull-down resistor.
AI_WS	26	LVTTL Schmitt 5 V tolerant	Input	I^2S Word Select Input. This pin has a weak internal pull-down resistor.
AI_SD	25	LVTTL Schmitt 5 V tolerant	Input	I^2S Data Input. This pin has a weak internal pull-down resistor.
AI_SPDIF/ DL2(IN)	28	LVTTL Schmitt 5 V tolerant	Input	S/PDIF Input/DSD Serial Left Channel 2 data input. This pin has a weak internal pull-down resistor.
ARC	40	Analog	Input	Audio Return Channel Input from HDMI. This pin can be left unconnected when not used.

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5.2.7. Configuration/Programming Pins

Pin Name	Pin	Type	Dir	Description
INT	3	LVTTL Open-drain 5 V tolerant 8 mA	Output	Interrupt Output. The INT pin can be programmed to be an open drain output (default) or a push-pull LVTTL output. The polarity of the INT pin can be set to negative (default) or positive asserted.
RESET#	16	LVTTL Schmitt 5 V tolerant	Input	Reset Pin. Active LOW. This pin has a weak internal pull-down resistor.
CSCL	67	LVTTL Schmitt Open-drain 5 V tolerant	Input	Configuration/Status I²C Clock. Chip configuration and status are accessed using this I²C port. This pin requires an external pull-up resistor. A suggested value is 4.7 kΩ or stronger. This pin has a weak internal pull-down resistor.
CSDA	68	LVTTL Schmitt Open-drain 5 V tolerant 8 mA	Input Output	Configuration/Status I²C Data. Chip configuration and status are accessed using this I²C port. This pin requires an external pull-up resistor. A suggested value is 4.7 kΩ or stronger. This pin has a weak internal pull-down resistor.
SPI_CS#/GPIO0	21	LVTTL Schmitt 5 V tolerant 8mA	Input	SPI Chip Select. Selected when the AO_SPDIF/DL2(OUT) pin is LOW during reset.
			Input Output	GPIO 0. Selected when the AO_SPDIF/DL2(OUT) pin is HIGH during reset. This pin has a weak internal pull-down resistor.
SPI_CLK/ GPIO1	22	LVTTL Schmitt 5 V tolerant 8mA	Input	SPI Clock. Selected when the AO_SPDIF/DL2(OUT) pin is LOW during reset.
			Input Output	GPIO 1. Selected when the AO_SPDIF/DL2(OUT) pin is HIGH during reset. This pin has a weak internal pull-down resistor.
SPI_TX/GPIO2	23	LVTTL Schmitt 5 V tolerant 8mA	Output	SPI Data Output. Selected when the AO_SPDIF/DL2(OUT) pin is LOW during reset.
			Input Output	GPIO 2. Selected when the AO_SPDIF/DL2(OUT) pin is HIGH during reset. This pin has a weak internal pull-down resistor.
SPI_RX/GPIO3	24	LVTTL Schmitt 5 V tolerant 8mA	Input	SPI Data Input. Selected when the AO_SPDIF/DL2(OUT) pin is LOW during reset.
			Input Output	GPIO 3. Selected when the AO_SPDIF/DL2(OUT) pin is HIGH during reset. This pin has a weak internal pull-down resistor.

5.2.8. Crystal Clock Pins

Pin Name	Pin	Type	Dir	Description
XTALIN	61	5 V tolerant LVTTL	Input	Crystal Clock Input. Generates internal system clock and allows LVTTL input. Frequency required is 26 MHz through 28.5 MHz. 27 MHz frequency is recommended. The system clock is used as the reference clock for the audio PLL and scaler PLL. It is also used for register access and interrupt processing.
XTALOUT	62	LVTTL	Output	Crystal Clock Output.

Note: The XTALIN pin can be driven at LVTTL levels by a clock (leaving XTALOUT unconnected) or connected through a crystal to XTALOUT.

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5.2.9. Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
IO_VDD5	1	Power	Power supply for CSCL, CSDA, CEC, CDSENSE, TX_DSCL, TX_DSDA, RX_DSDA, RX_DSCL and RX_HPD/CBUS pins.	5.0 V
MCAP33	2	Power	Capacitor for Internal Regulator.	3.3 V
RX_AVDD10	4, 14	Power	TMDS Rx Analog 1.0 V Power Supply.	1.0 V
RX_AVDD33	5	Power	TMDS Rx Analog 3.3 V Power Supply.	3.3 V
TX_PVDD10	43	Power	TMDS Tx PLL Analog 1.0 V Power Supply.	1.0 V
TX_AVDD10	46, 51	Power	TMDS Tx Analog 1.0 V Power Supply.	1.0 V
DVDD10	15, 17, 18, 20, 38, 41, 54, 55, 56, 57, 58, 65	Power	Digital Logic Power Supply.	1.0 V
VP_AVDD10	59	Power	Video PLL Power Supply.	1.0 V
AP_AVDD10	64	Power	Audio PLL Power Supply.	1.0 V
IO_VDD33	19	Power	I/O Power Supply.	3.3 V
IO_APVDD33	63	Power	Audio PLL I/O Power Supply.	3.3 V
TX_GND	42	Ground	TMDS Tx Ground.	Ground
IO_APGND	60	Ground	Audio PLL I/O Ground.	Ground
GND	ePad (bottom of package)	Ground	Ground. The ePad ***must*** be soldered to ground.	Ground

5.2.10. Reserved Pins

Pin Name	Pin	Type	Description	Supply
RSVDNC	66	Reserved	Do not connect.	—
RSVDL	69	Reserved	Reserved. Must be tied to ground.	Ground

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6. Feature Information

6.1. I²C and SPI Interfaces

6.1.1. E-DDC/I²C Interface

The HDCP protocol requires the video transmitter and video receiver to exchange values. The transmitter reads the EDID data in the receiver to ascertain its capabilities. These values are exchanged over the DDC channel of the HDMI interface. The E-DDC channel follows the I²C serial protocol. Both the HDMI receiver and transmitter ports of the SiI9612 device feature their own separate E-DDC buses.

6.1.1.1. HDMI Receiver E-DDC Interface

The HDMI receiver port of the SiI9612 device has a connection to the E-DDC bus with the slave address of 0x74 for HDCP authentication, and 0xA0 for EDID data retrieval by the upstream transmitter. The I²C read operation is shown in Figure 6.1, and the write operation in Figure 6.2.

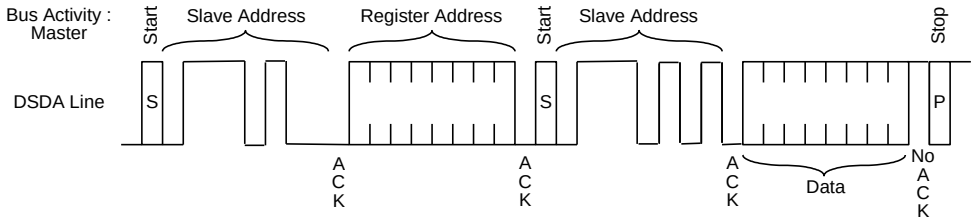

Figure 6.1. DDC Byte Read

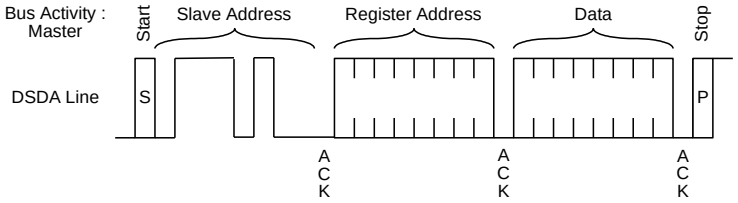

Figure 6.2. DDC Byte Write

Multiple bytes can be transferred in each transaction, regardless of whether they are reads or writes. The operations are similar to those in the two figures above, except that there is more than one data phase. An ACK follows each byte except the last byte in a read operation. Byte addresses increase with the least-significant byte transferred first, and the most-significant byte last. See the I²C Specification for more information.

There is also a Short Read format that can be performed during the third phase of HDCP authentication. It is designed to improve the efficiency of Ri register reads that must be done every two seconds while encryption is enabled. Figure 6.3 shows this transaction. There is no register address phase (only the slave address phase), because the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP condition on any preceding I²C transaction.

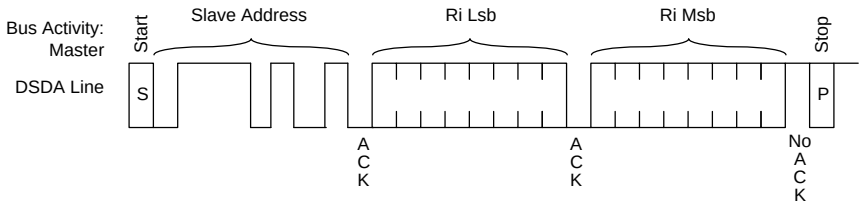

Figure 6.3. Short Read Sequence

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6.1.1.2. HDMI Transmitter E-DDC Interface

The SiI9612 HDMI transmitter port interfaces with the E-DDC bus through an I²C master controller. The DDC master supports the I²C transactions specified by the VESA Enhanced Display Data Channel Standard. The DDC master complies with the 100 kHz standard mode timing of the I²C Specification and supports slave clock stretching, as required by E-DDC. Figure 6.4 shows the supported transactions and timing sequences.

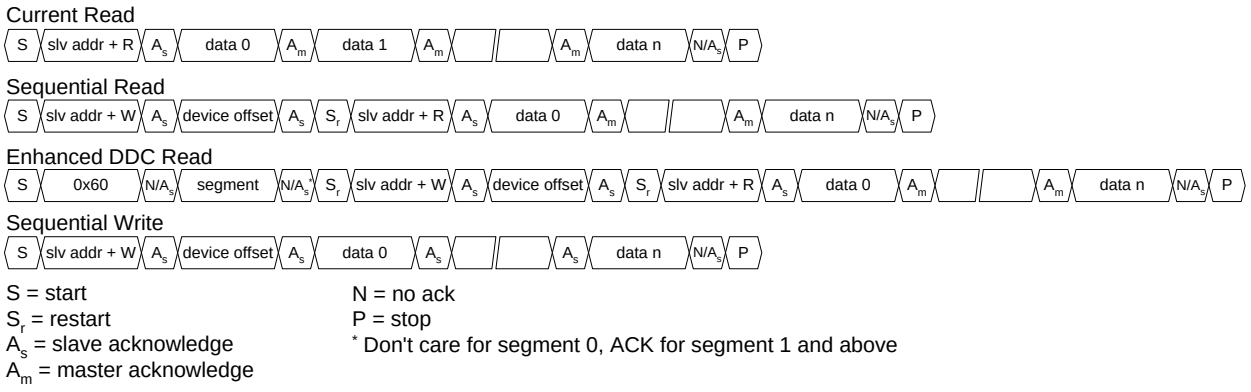

Figure 6.4. DDC Master I²C Supported Transactions

6.1.2. Local I²C Interface

The SiI9612 video processor has a third I²C port accessible only to the controller in the display device. It is separate from the E-DDC bus and is a slave device. The local I²C interface on SiI9612 pins CSCL and CSDA is a slave interface that can run up to 400 kHz. This bus is used to configure and control the video processor by reading and writing to necessary registers.

The device registers are accessed using 16-bit addresses. Figure 6.5 illustrates the bus activity on the CSDA line when writing to a device register, and Figure 6.6 illustrates the same when reading a device register. In both read and write cycles, after the master transmits the device address and receives an acknowledgment from the slave, it sends two bytes, which represent the address of the register it wants to read or write. These two bytes make up the high and low bytes of the register address. The rest of the bus cycle follows the same format as transactions using an 8-bit register address. For example, to write to register 0x1008 of the HDMI receiver, the master would transmit 0x10 for the high address byte and 0x08 for the low address byte.

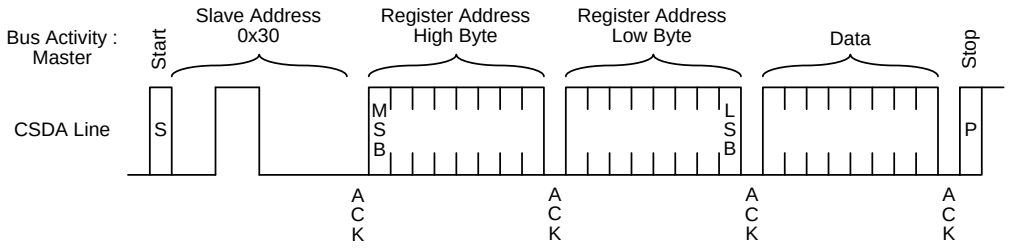

Figure 6.5. Register Write Cycle on Local I²C

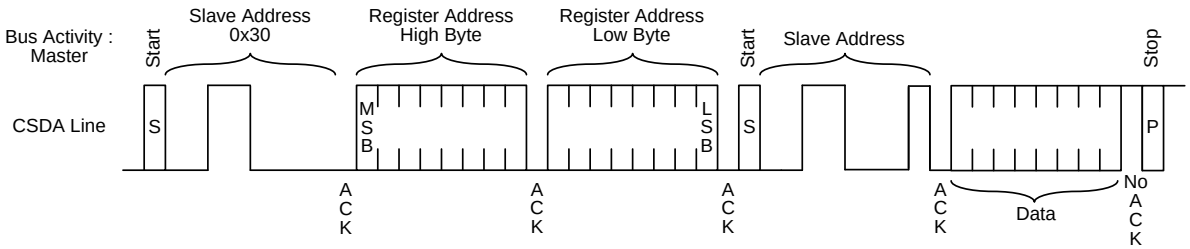

Figure 6.6. Register Read Cycle on Local I²C

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Multibyte transfers are supported. The operations are similar to those described above. The internal address pointer is advanced automatically after every transfer of a byte.

The device address of the local I²C interface can be set to one of two values by strapping the AO_MUTE pin LOW or HIGH at reset. Table 6.1 shows the device address selected for each state of the AO_MUTE pin at reset.

Table 6.1. Control of Local I²C Device Address with AO_MUTE Pin

Device Address	AO_MUTE = LOW	AO_MUTE = HIGH
Local I²C	0x30	0x32

6.1.3. Video Requirement for I²C Access

The SiI9612 video processor does not require an active video clock to access its registers from either the E-DDC port or the local I²C port. Read/Write registers can be written and then read back. Read-only registers that provide values for an active video or audio stream return indeterminate values if there is no video clock and no active sync.

Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

6.1.4. Local SPI Serial Interface

The SPI serial interface is a simple four-wire synchronous serial interface with unidirectional data lines. The host CPU drives clock, chip select, and serial transmit data to the SPI slave device. It also receives serial data from the SPI slave device. By using multiple chip-enables and tying the receive data lines together, it is possible to connect multiple SPI slave devices to a single host CPU as shown in Figure 6.7 and Figure 6.8. The maximum clock frequency is 10 MHz.

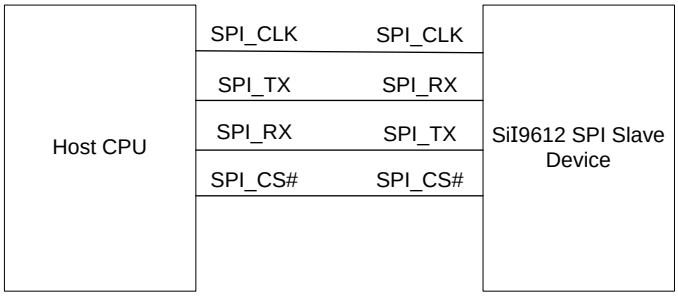

Figure 6.7. SPI Serial Connection Example: Host ↔ Single SPI Slave Device

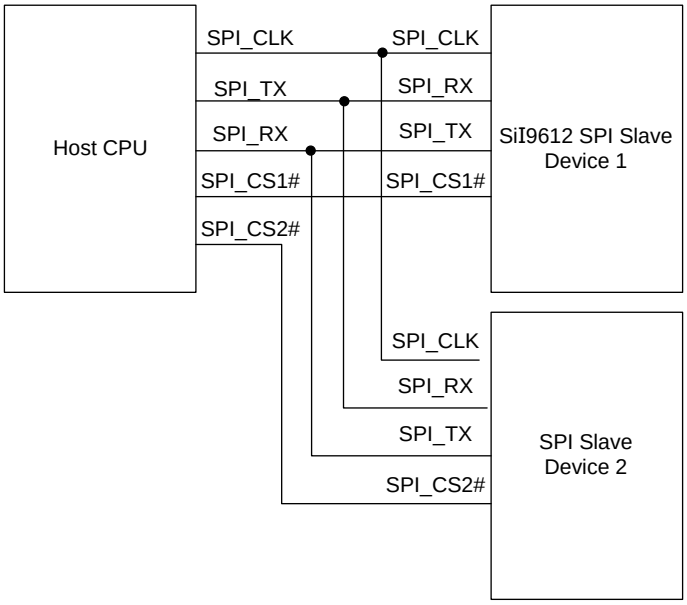

Figure 6.8. SPI Serial Connection Example: Host ↔ Dual SPI Slave Devices

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6.1.4.1. Write Operation

The following description of a write operation is from the perspective of the host controller as shown in Figure 6.9.

First, the host CPU asserts the SPI_CS# line LOW to indicate the start of a transfer. Then it sends 15 address bits (MSB first) on the SPI_TX line, followed by a single R/W bit (0 = write). For a write operation, the host CPU sends *N* bytes of write data one byte at a time (MSB first). The order of bits on the SPI_TX line is 7–0, 15–8, 23–16, and so on. When more than one byte is written, the address is incremented automatically in the SPI slave device. The maximum number of bytes that may be written in a single transaction is not limited by the bus protocol, but may be limited by the slave device.

At the end of the transaction, SPI_CS# is deasserted to indicate the end of the transfer. If SPI_CS# is deasserted too early, the slave device aborts the transfer, and the results may be undefined.

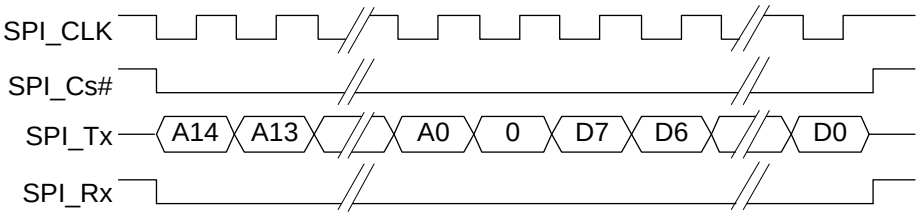

Figure 6.9: SPI Serial Write Operation

Note: Signal names are as seen at the host side of the interface.

6.1.4.2. Read Operation

The following description of a read operation is from the perspective of the host controller as shown in Figure 6.10 below.

First, the host CPU asserts the SPI_CS# line LOW to indicate the start of a transfer. Then it sends 15 address bits (MSB first) on the SPI_TX line, followed by a single R/W bit (1 = read). For a read operation, the host CPU must poll the SPI_RX line while holding the clock pin HIGH, until the slave device drives the SPI_RX line HIGH to indicate data is ready. The host may then start reading *N* bytes of data one byte at a time (MSB first). The order of bits on the serial line is 7–0, 15–8, 23–16, and so on.

Similar to the write operation, when more than one byte is read, the address is incremented automatically in the SPI slave device. The maximum number of bytes that may be read in a single transaction is not limited by the bus protocol, but may be limited by the slave device. Note that the serial clock does not toggle in the pause between sending the address and receiving read data. At the end of the transaction, SPI_CS# is deasserted to indicate the end of the transfer. If SPI_CS# is deasserted too early, the slave device aborts the transfer, and the results may be undefined.

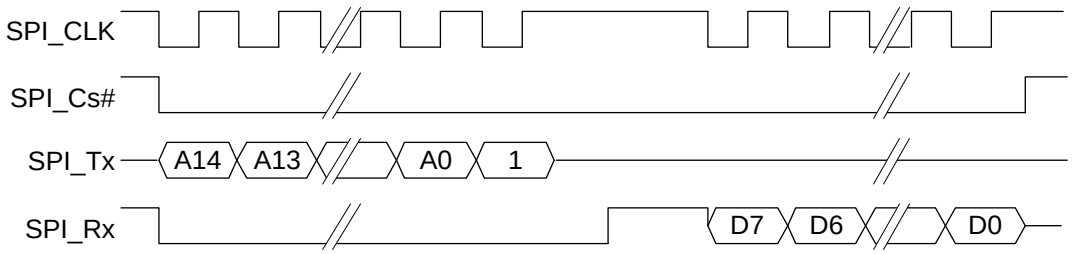

Figure 6.10: SPI Serial Read Operation

Note: Signal names are as seen at the host side of the interface.

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7. Package Information

7.1. ePad Requirements

The SiI9612 video processor is packaged in a 76 pin, 9 mm × 9 mm MQFN package with ePad that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 5.38 mm × 5.38 mm ± 0.15 mm. Soldering the ePad to the ground plane of the PCB is required to meet package power dissipation requirements at full-speed operation, and to correctly connect the chip circuitry to electrical ground. To avoid the possibility of electrical shorts, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package standoff when mounting the device also needs to be considered. For a nominal standoff of approximately 0.1 mm, the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 7.1 on the next page shows the package dimensions of the SiI9612 video processor.

7.2. PCB Layout Guidelines

Refer to Lattice Semiconductor document *PCB Layout Guidelines: Designing with Exposed Pads* (Lattice Semiconductor Documents on page 51) for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

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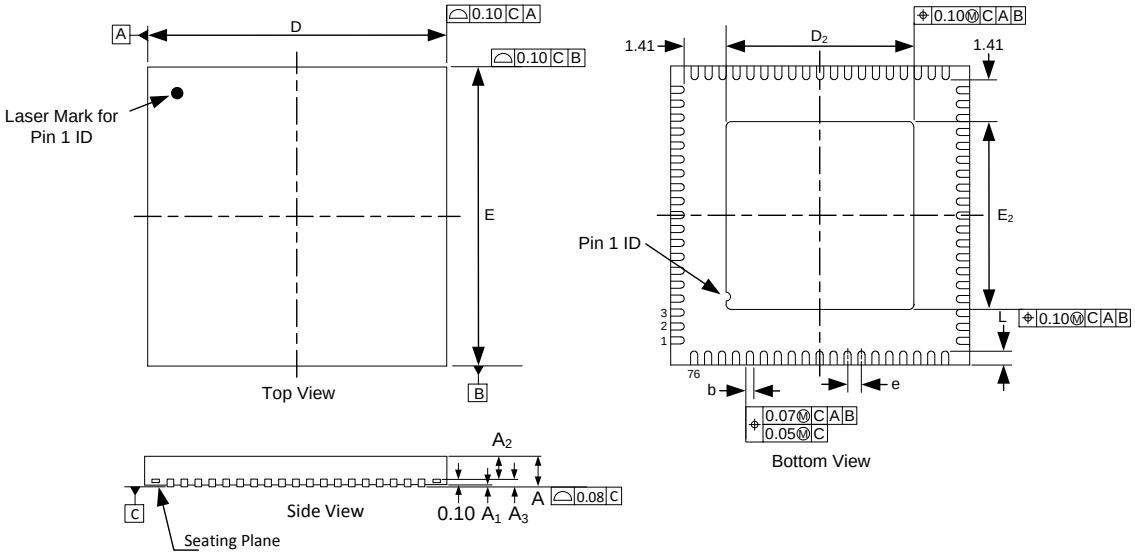
7.3. Package Dimensions

This figure is not to scale.



JEDEC Package Code MO-220 (Dimensions in mm)

Symbol	Min	Typ	Max
A	0.80	0.85	0.90
A_1	0.00	0.02	0.05
A_2	—	0.65	0.70
A_3	0.20 REF		
b	0.15	0.20	0.25
D	9.00 BSC		

Symbol	Min	Typ	Max
D_2	5.23	5.38	5.53
E	9.00 BSC		
E_2	5.23	5.38	5.53
L	0.30	0.40	0.50
e	0.40 BSC		

Figure 7.1. Package Diagram

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7.4. Marking Specification

Figure 7.2 and Figure 7.3 show the markings of the SiI9612 package. Refer to Figure 7.1 on page 49 for specifics.

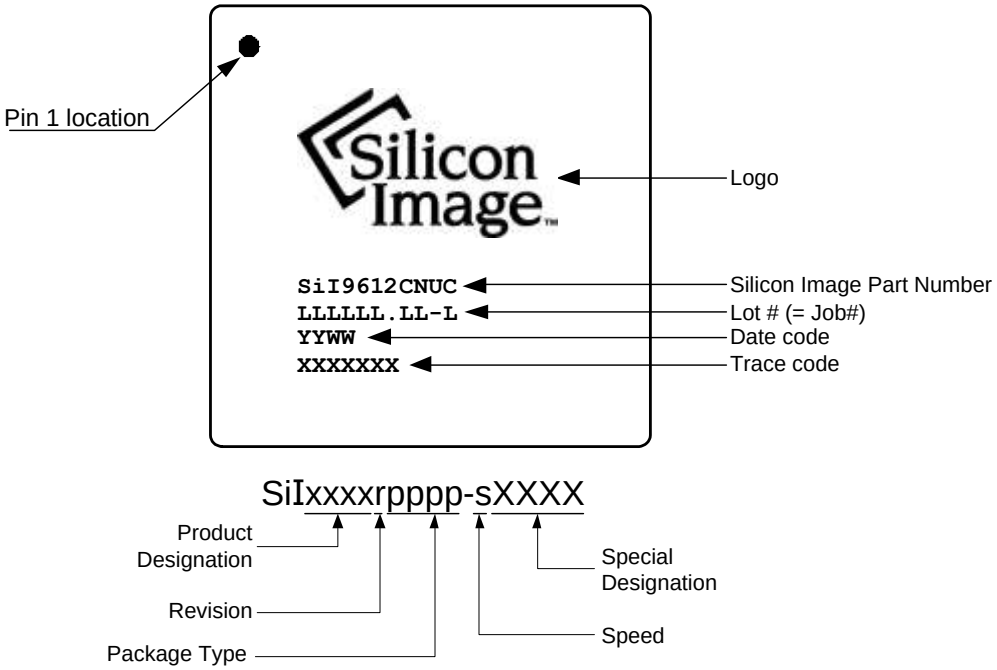

Figure 7.2. Marking Diagram

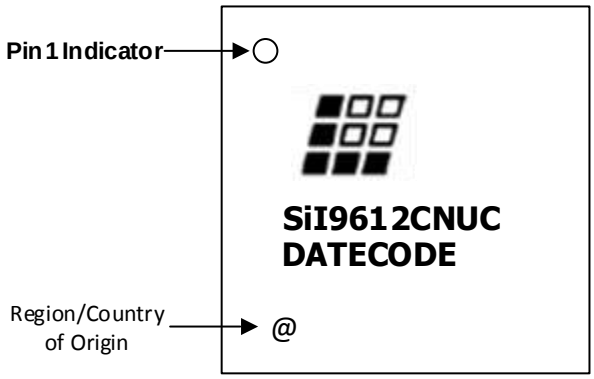

Figure 7.3. Alternate Topside Marking

7.5. Ordering Information

Production Part Numbers:

TMDS Clock Range	Part Number
25 MHz – 300 MHz	SiI9612CNUC

The universal package may be used in lead-free and ordinary process lines.

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References

Standards Documents

This is a list of standards abbreviations appearing in this document, and references to their respective specifications documents.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface,* Revision 1.4, HDMI Consortium; June 2009
HCTS	*HDMI Compliance Test Specification,* Revision 1.3c, HDMI Consortium; July 2008
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.3, Digital-Content Protection, LLC; December 2006
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; February 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA; June 2001
CEA-861	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; January 2001
CEA-861-B	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002
CEA-861-D	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; July 2006
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA; March 2004
MHL	*MHL (Mobile High-definition Link) Specification*, Version 2.0, MHL, LLC, February 2012

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
DVI	http://www.ddwg.org
HDCP	http://www.digital-cp.com
HDMI	http://www.hdmi.org
MHL	http://www.mhlconsortium.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-PR-1069	*SiI9616/SiI9612 Programmer's Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer's Reference*
SiI-AN-0129	*PCB Layout Guidelines: Designing with Exposed Pads*

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

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Revision History

Revision C, April 2017

Marking spec changed as per PCN13A16. Added Figure 7.3. Alternate Topside Marking.

Revision B, February 2016

Updated to latest template.

Revision B, October 2013

Updated the Direct Stream Digital Input and the One-bit Audio Output sections.

Revision A, February 2013

First production release.

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