GSV6715

4 In to 1 Out HDMI 2.1/DisplayPort 1.4 to HDMI 2.1 Mixed Switch with Embedded MCU

April, 2022

Preliminary Product Specification

1. General Description

1.1 General Information

Gscoolink GSV6715 is a high-performance, low-power 4 In to 1 Out HDMI 2.1/DisplayPort 1.4 to HDMI 2.1 mixed switch. By integrating enhanced microcontroller based on RISC-V, GSV6715 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane), HDMI Receiver and HDMI Transmitter supports up to 48Gbps (FRL, 12G/4Lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV6715 can directly map its one receiver to USB Type-C interface, and Alternate DisplayPort for Type-C can be supported for Type-C to HDMI application. The superior architecture of GSV6715 provides economical smaller footprint solutions using QFN124, targeting applications of TV/Monitor/Sound bar/Stream box and KVM.

GSV6715 supports all DisplayPort SDP packets and DSC stream pass-through to HDMI output. HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6715 for its all DisplayPort and HDMI ports in HDMI 2.0 and FRL mode. Color Space Conversion is supported at HDMI Tx in HDMI 2.0 mode. Flexible implementations of Audio Insertion, Audio Extraction and SPDIF to I2S conversion features are supported in GSV6715. Embedded CEC and eARC Rx engine enable downstream ARC/eARC to I2S and SPDIF audio extraction features.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.1, such as 8K@60Hz, 8K@30Hz, 4K@120Hz, 480i@60Hz.

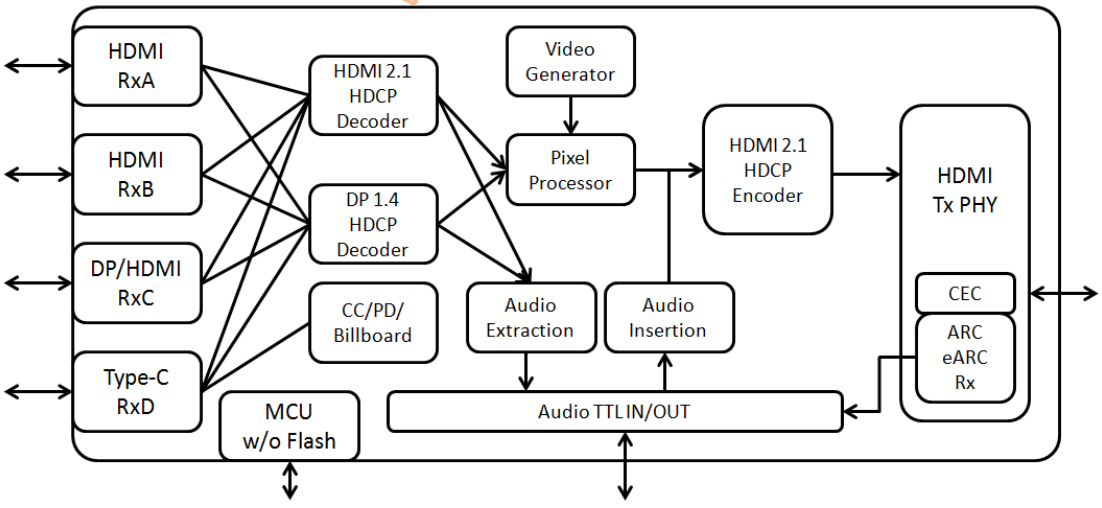


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Adaptive Sync/FreeSync/G-Sync to HDMI VRR output conversion
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K120 format
- Support Forward Error Correction (FEC)
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)
- Support DSC bypass to HDMI output
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

1.2.2 HDMI Receiver

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b

- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support Forward Error Correction (FEC)
- Support DSC pass-through for compressed input timing
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 HDMI Transmitter

- Compliant with HDMI 2.1a, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support DSC encoded stream pass-through from HDMI/DP input
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins
- 3D format support of frame packing, side-by-side, top-and-bottom
- Support eARC Rx to I2S/SPDIF audio extraction in HDMI 2.1a

1.2.4 USB Type-C DisplayPort Alternative Mode Receiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function
- Support Billboard in USB 2.0

1.2.5 Audio Input/Output

- I2S and SPDIF Audio Extraction from DisplayPort Rx/HDMI Rx/Type-C Rx
- I2S and SPDIF Audio Extraction from downstream ARC /eARC
- I2S/SPDIF Audio Insertion to HDMI Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction and Insertion
- SPDIF to I2S Conversion using single Bi-directional TTL bus

1.2.6 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU and External Flash
- External pins of Flash QSPI interface
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 HDMI 3 Input, Type-C Alt-Mode 1 Input

RxA/RxB/RxC are configured as HDMI Rx Input, RxD is configured as Type-C Alt-Mode (DisplayPort) Rx Input. This mode is applicable for monitor application. In this application, Type-C Rx can maintain its stream with one HDMI Rx for fast hot-swap without HPD toggling during input switch.

Within bandwidth limitation, GSV6715 can keep input stream consistent and intact, while dynamically switch output between FRL and HDMI 2.0 mode for the best compatibility. For example, when FRL12G/4Lane 4K@60Hz timing is input, GSV6715 can convert to HDMI 2.0 or FRL 6G/3Lane, FRL 6G/4Lane, FRL 8G/4Lane, FRL 10G/4Lane, FRL 12G/4Lane as output. During HDMI output mode switch, HDMI input stream will not be disturbed.

GSV6715 can also support fixed output FRL rate, regardless of HDMI input mode. For example, when HDMI 2.0 4K@30Hz is input, GSV6715 can convert it to FRL 10G/4Lane output. And when FRL 8G/4Lane 4K@120Hz is input, GSV6715 can still maintain FRL 10G/4Lane output with timing conversion.

Meanwhile, Audio extraction can be applicable if required.

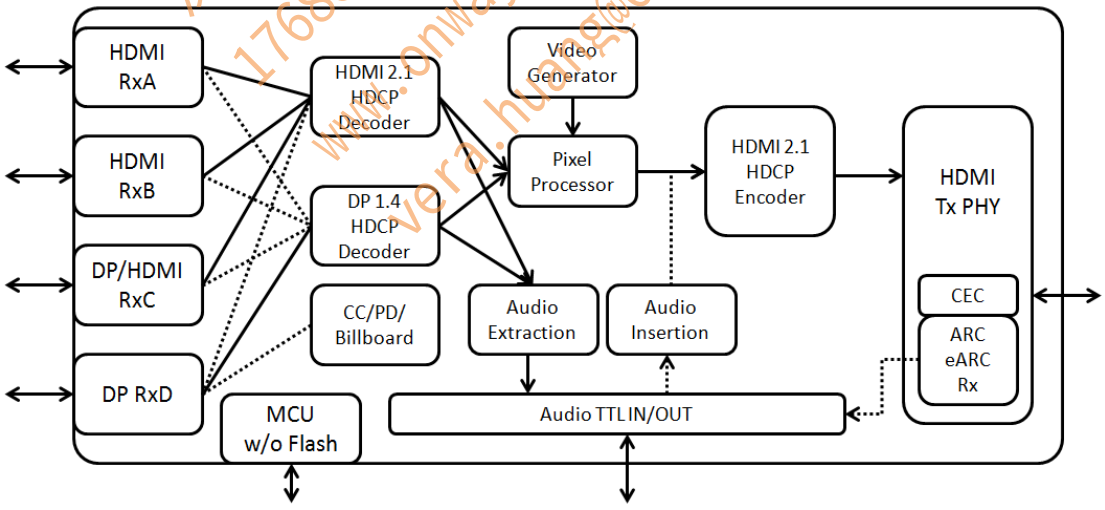


Figure 2. Input Switch Between Different Inputs

1.3.2 HDMI 2 Input, DisplayPort 1 Input, Type-C 1 Input

RxA/RxB are configured as HDMI Rx Input, RxC is configured as DisplayPort Rx Input, RxD is configured as Type-C Alt-Mode DisplayPort Rx Input. This would applicable for monitor application.

I2S/SPDIF audio stream can be inserted into HDMI Tx if required.

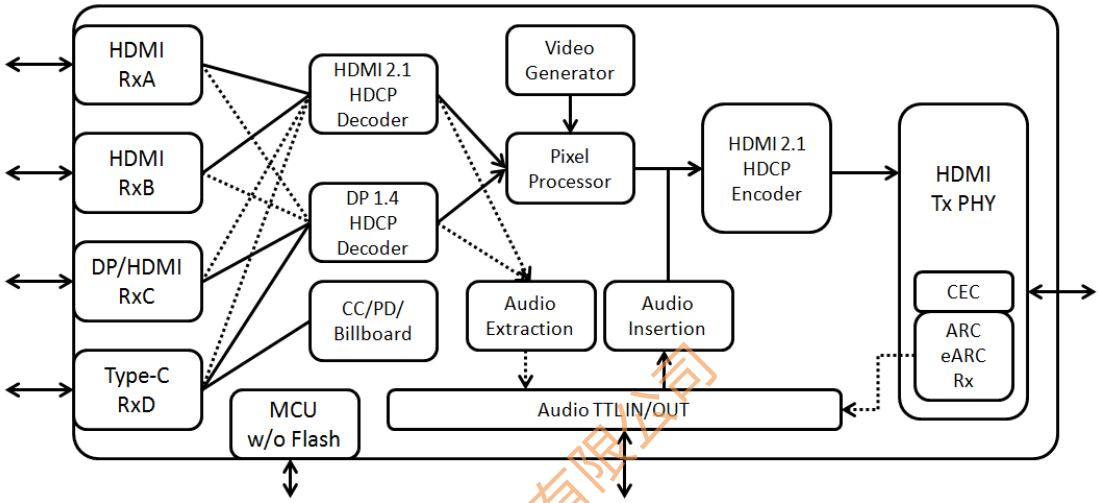


Figure 3. Audio Insertion Application

1.3.3 Audio Return to Audio Extraction

With embedded CEC engine, GSV6715 HDMI Tx can support ARC return channel defined in HDMI 1.4b specification. GSV6715 can convert SPDIF in ARC return stream to both SPDIF and I2S TTL output on Audio Bus.

With embedded eARC Rx engine, GSV6715 HDMI Tx can support eARC return channel defined in HDMI 2.1a specification. GSV6715 can convert SPDIF in eARC return stream to both SPDIF and I2S TTL output on Audio Bus.

HDMI Tx differential pairs can output FRL/HDMI 2.0 to downstream while ARC/eARC feature is enabled.

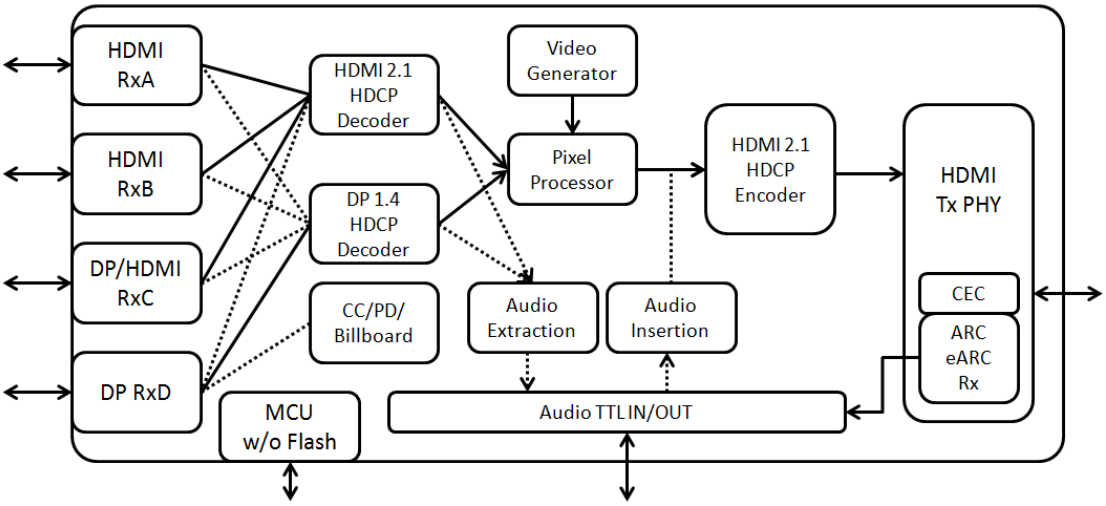


Figure 4. Audio Return Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Output	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Output	I2S Data, 5/6 channels
AUD_D3	SDATA[3]	Output	I2S Data, 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

For HBR application, SPDIF is also capable of sending out with 4 pins.

Table 3. HBR Audio Extraction in SPDIF

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels
AUD_D1	SPDIF[1]	Output	SPDIF Data[1], 3/4 channels
AUD_D2	SPDIF[2]	Output	SPDIF Data[2], 5/6 channels
AUD_D3	SPDIF[3]	Output	SPDIF Data[3], 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel, 1/2 channels

2. Pin Description

2.1 Pin Diagram

QFN124 Pin definition is defined as below.

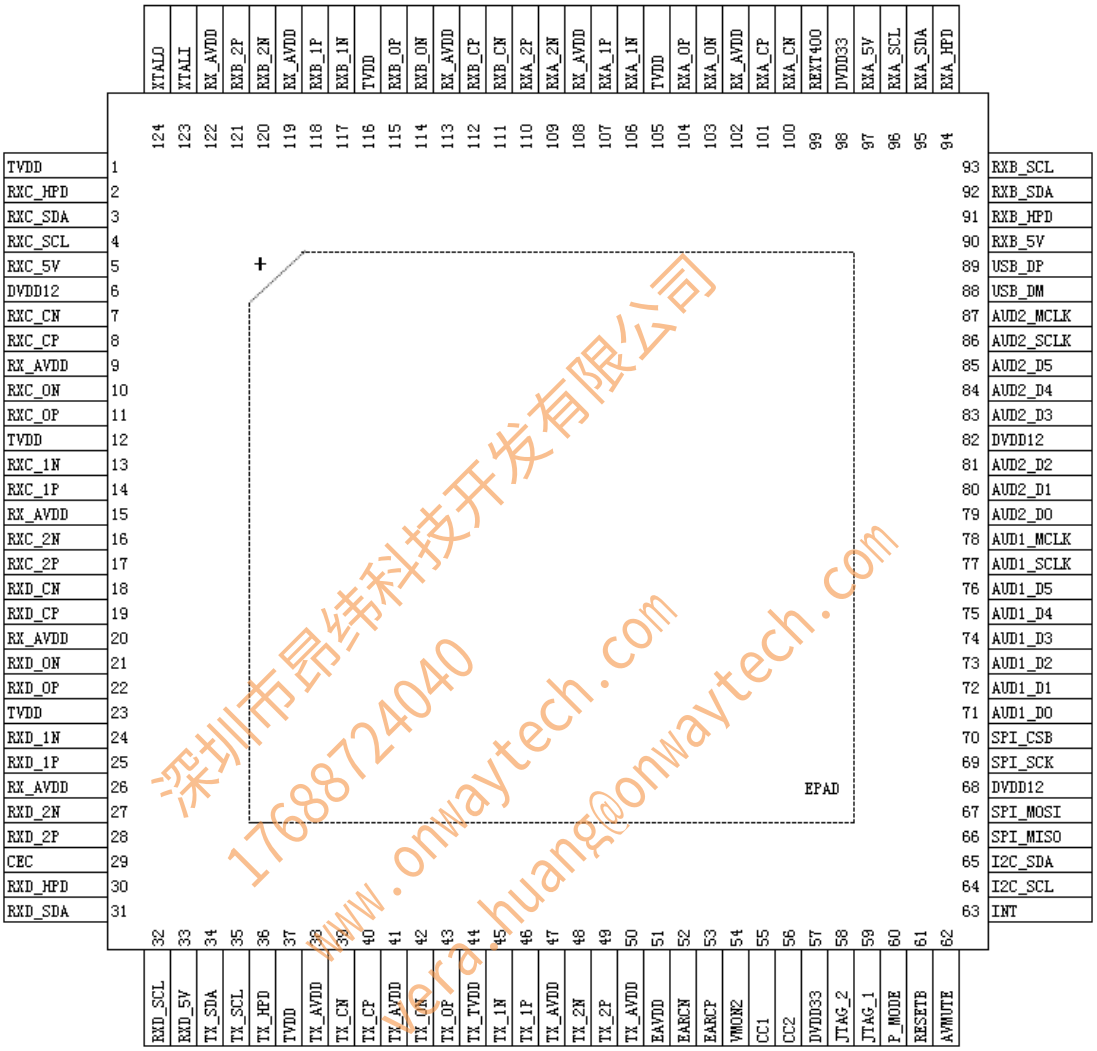


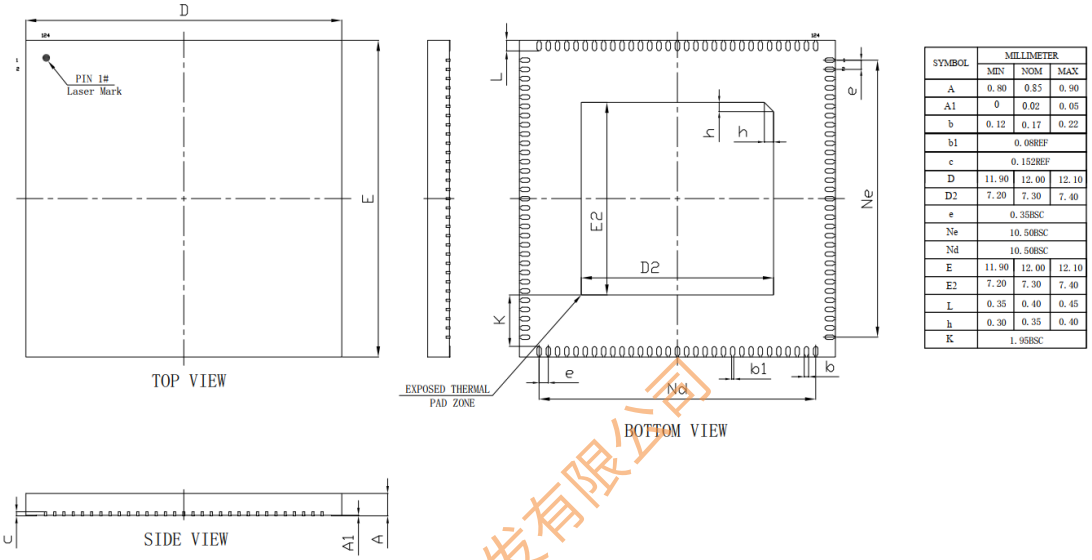
Figure 5. GSV6715 QFN124 Pin Diagram

2.2 QFN124 Pin Description

Table 8. QFN124 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI RxA Pins			
RXA_5V	I	97	HDMI: RXA 5V Detection PAD DP: RXA DP Detection PAD

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.12	0.17	0.22
b1		0.08REF	
c		0.152REF	
D	11.90	12.00	12.10
D2	7.20	7.30	7.40
e		0.35BSC	
Ne		10.50BSC	
Nd		10.50BSC	
E	11.90	12.00	12.10
E2	7.20	7.30	7.40
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		1.95BSC	

Figure 12. Package Dimensions (QFN124)

5. Ordering Guide

Table 12. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6715	−20°C to +85°C	124QFN	Tray