GSV1016

HDMI2.0 HDCP1.4 Transmitter with
TTL/LVDS Input and Audio Insertion

September, 2019

PRODUCT SPECIFICATION

1 General Information

1.1 General Information

The GSV1016 is a HDMI1.4 compatible TX transmitter with LVDS/TTL data bus, and supports HDCP 1.4. For audio extraction and insertion, GSV1016 can support up to 8-channel I2S/2-channel S/PDIF/TDM.

The HDMI input maximum processing pixel clock frequency is 300MHz which means the video resolution can support up to 4kx2k@30Hz 4:4:4 8-bit. The maximum processing audio sample frequency is 8-channel 192K Hz for non-compression timing.

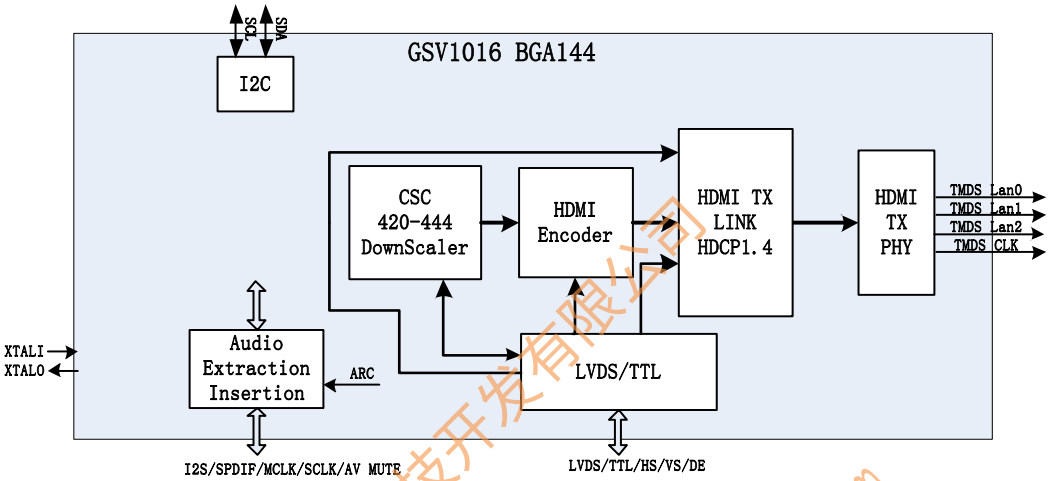


Figure 1 top diagram

Internal video processing supports CSC/ Dither/ 420<->444 conversion/ Downscaler/ Deinterlacer/ LVDS and TTL Pin Mapping. Figure 2 is its diagram.

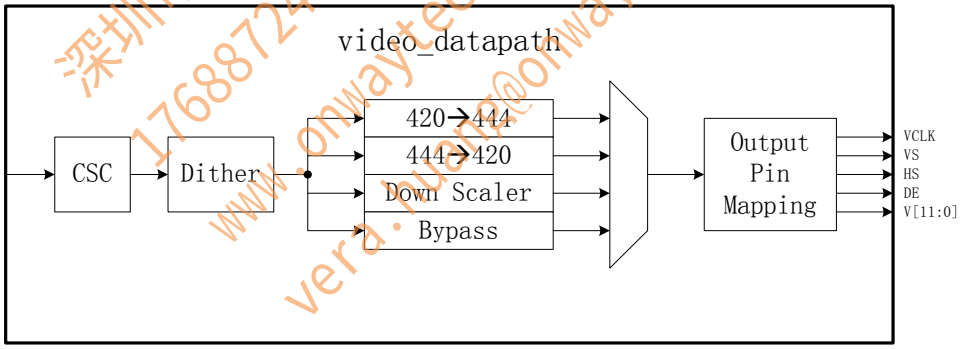


Figure 2 video datapath diagram

Audio TTL input pins support audio format listed in Table 1.

Table 1 supported audio format

Packet ID	Packet Type	Sample Frequency or Frame Rate		
		32.0, 44.1, 48.0, 88.2, 96.0, 176.4, and 192.0 kHz	256.0, 352.8, 384.0, 512.0, 705.6, 768.0 kHz	64.0 and 128.0 kHz
0x02	Audio Sample (L-PCM and IEC 61937 compressed formats)	Y	N	Y
0x07	One Bit Audio Sample Packet	Y	N	N
0x08	DST Audio Packet	Y	N	N
0x09	High Bitrate Audio Stream Packet (IEC 61937)	N	Y	N

An internal Clock Generator can be used to generate 4 independent output clocks, which will greatly remove complexity of using dedicated clock device.

1.2 Features

1.2.1 HDMI TX Transmitter

- Compliant with HDMI2.0b, HDMI1.4b
- Compliant with HDCP1.4
- Data rate up to 18Gbps
- Programmable HDMI Tx input swing, slew-rate, pre-emphasis
- AC-coupling capable
- UDP bus to support the combination of video/audio/info-frames
- Color Space Converter supports any conversion between different color spaces
- HDR supported (HDR10/HDR12/Dolby Vision/HLG)
- 5V tolerance on DDC/HPD/CEC
- Up to 4 channel clock generators, ranging 25MHz~600MHz

1.2.2 Multi-Port LVDS Receiver

- Bi-directional LVDS, supports video format up to 4K 30 444
- Compatible with series FPGAs' LVDS standard (15 pairs in maximum)
  - SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable input phase
  - Data rate up to 1.5Gbps per lane
  - Differential HS/VS/DE available
  - Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Receiver
  - Data rate up to 1.5Gbps per lane

1.2.3 Compatible TTL Receiver

- 48bit TTL Video Receiver
  - TTL Schmitt trigger receiver and CMOS receiver selectable
  - SDR/DDR Clock Input available with 0 degree or 90 degree
  - Data rate up to 300Mbps per lane
  - HS/VS/DE available
  - Embedded SAV/EAV mode supported
  - 1.8/2.5/3.3V VCCO compatible.

1.2.4 Audio Input

- SPDIF/I2S/HBR/DSD/TDM Audio Insertion

1.3 Chip Application Modes

1.3.1 HDMI 1.4 TX with LVDS/TTL input

The LVDS/TTL input and Audio TTL input can be combined in HDMI Tx Encoder to generate HDMI 1.4 timing out.

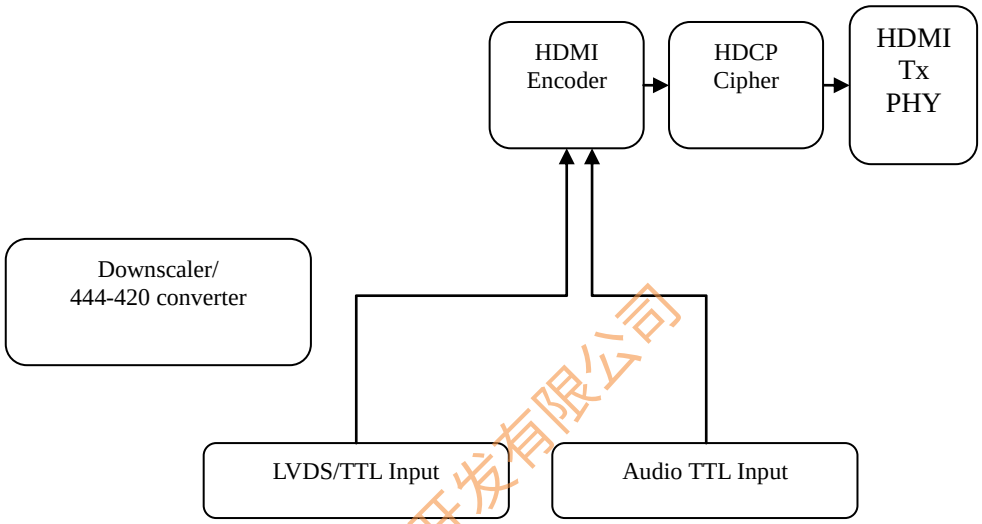


Figure 3 HDMI 1.4 TX with LVDS/TTL input

1.3.2 HDMI 1.4 TX with LVDS/TTL input with CSC

The LVDS/TTL input can convert color space internally before route to HDMI Encoder. In this mode, with different color space from LVDS/TTL input, HDMI Tx can generate a universal color space.

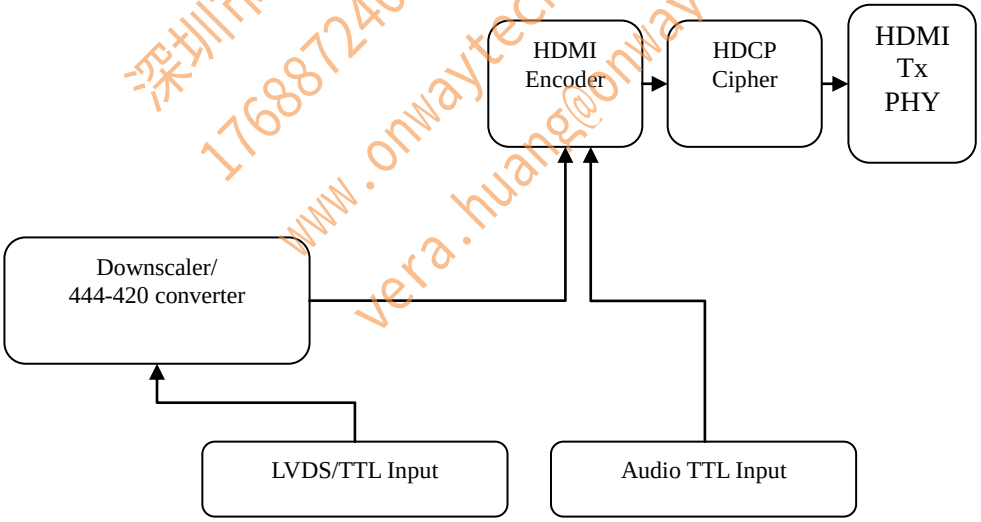


Figure 4 HDMI 1.4 TX with LVDS/TTL input with CSC

1.3.3 HDMI 1.4 TX with LVDS/TTL input using UDP mode

Patented UDP mode is used to drive the input video/audio stream in LVDS/TTL bus to HDMI input to minimize the pin number.

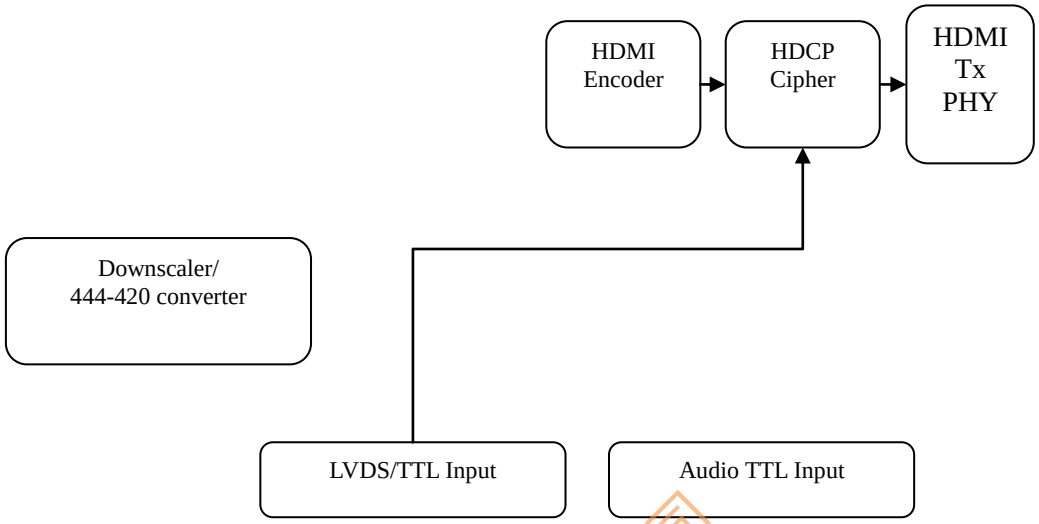


Figure 5 HDMI 1.4 TX with LVDS/TTL input using UDP mode

1.4 Audio Bus Input Capability

When Audio Bus is set to Input, either I2S or SPDIF can be selected as audio input source. It should be noted that MCLK must be externally fed into GSV chip in I2S audio insertion mode.

For SPDIF input, GSV series chip can detect Sampling Frequency and automatically update it in Channel Status with GSV software. For I2S input, software designer needs to indicate the current input sampling frequency in software.
Common application modes are listed.

Table 2. Stereo I2S Input

Pin Name	Alias	Direction	Description
AP0	SDATA[0]	Input	I2S Data, default stereo channels
AP5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

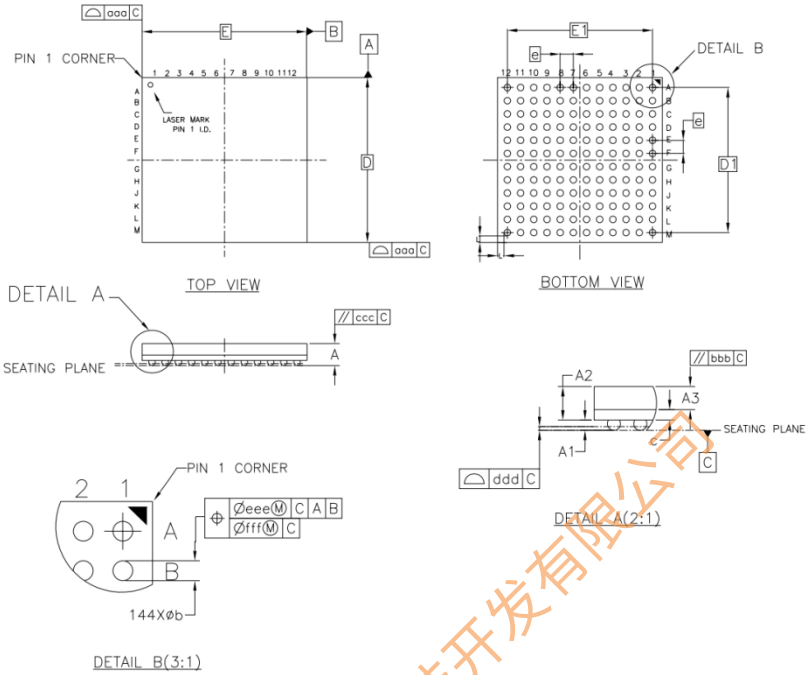
Table 3. SPDIF Input

Pin Name	Alias	Direction	Description
AP0	SPDIF	Input	SPDIF channel

Table 4. 8 channel I2S Input

Pin Name	Alias	Direction	Description
AP0	SDATA[0]	Input	I2S Data, default stereo channels
AP1	SDATA[1]	Input	I2S Data, 2/3 channels
AP2	SDATA[2]	Input	I2S Data, 4/5 channels
AP3	SDATA[3]	Input	I2S Data, 6/7 channels
AP5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

5 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.25	1.33	1.41
A1	0.26	0.31	0.36
A2	1.01	1.02	1.11
A3		0.70 BASIC	
c	0.28	0.32	0.36
D	9.90	10.00	10.10
D1		8.80 BASIC	
E	9.90	10.00	10.10
E1		8.80 BASIC	
e		0.80 BASIC	
b	0.35	0.40	0.45
L		0.40 REF	
aaa		0.10	
bbb		0.10	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	

Figure 25. Package Dimensions (BGA144)

6 Ordering Guide

Table 32. Ordering Infomation

Part Number.	Temperature Range	Package Description	Packing Type
GSV1016	−20 ℃ to +85 ℃	BGA144, 0.8 mm ball pitch, 10 mm x 10 mm outline	Tray