GSV2221

DisplayPort 1.4 MST to HDMI 2.0/DP/eDP Converter with Embedded MCU

November, 2024

Preliminary Product Specification

1. General Description

1.1 General Information

GSCoolink GSV2221 is a high-performance, low-power, USB Type-C Alternate Mode DisplayPort 1.4 MST to HDMI 2.0/DP/eDP converter with DSC decoder. By integrating enhanced microcontroller, GSV2221 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort MST Receiver supports up to 32.4Gbps (HBR3, 4-lane) and 2 compressed or uncompressed streams output through the HDMI Transmitter that supports up to 18Gbps (TMDS, 6Gbps, 3Lane), or DP/eDP Transmitter that supports up to 32.4Gbps (HBR3, 4-lane). Integrated Power Delivery 3.0 controller handles Type-C CC interface for USB power management and DisplayPort mode entry. The superior architecture of GSV2221 provides economical smaller footprint solutions using QFN88, targeting video conference applications such as applications of Type-C Docking, Type-C dongle and DP to HDMI cable.

GSV2221 can transport more than 2 compressed or uncompressed video/audio streams, and 2 streams can be selected for the two TX ports. Two independent DSC video decoders can be supported for TX ports, and each DSC decoder is available for up to 4K 60Hz 444 color formats with 2 slices.

GSV2221 supports all DisplayPort SDP packets pass-through to HDMI output. HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV2221 for both DisplayPort and HDMI TMDS mode. Color Space Conversion is supported at HDMI Tx in TMDS mode.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.0, such as 4K@60Hz, 4K@30Hz, 480i@60Hz.

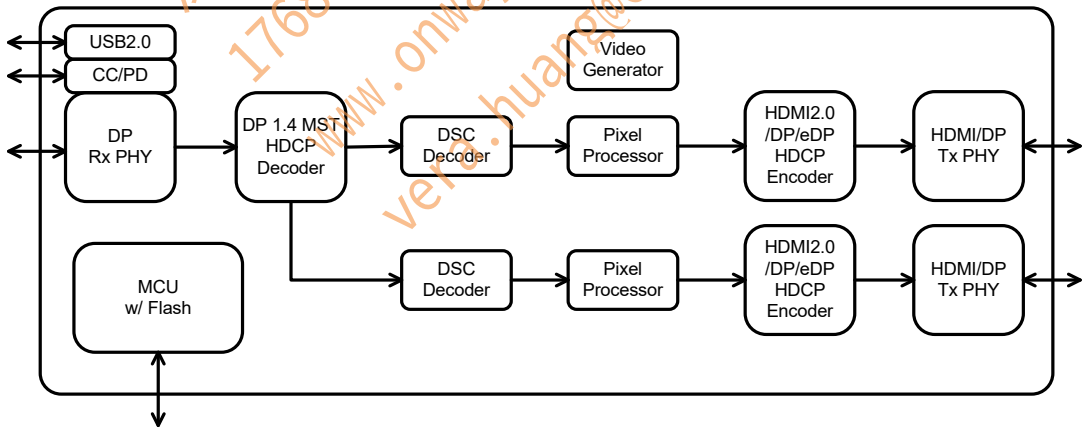


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128

0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Support SST/MST transport streams
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Horizontal Blanking Expansion
- Support Forward Error Correction (FEC)
- Support DSC decoder for both SST and MST
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)

1.2.2 HDMI Transmitter

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 18Gbps (TMDS 6Gbps and 3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS
- Support Color Space Converter in HDMI 2.0 mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.3 DisplayPort/eDP Transmitter

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Support SST transport stream

1.2.4 USB Type-C Interface

- USB Power Delivery 3.0 Compliant controller
- 6 Configuration Channels (CC) with built-in Rp/Rd resistors
- Dual Role Power Port (DRP)
- Fast Role Swap
- USB 2.0 full-speed billboard enumeration

1.2.5 DSC Decoder

- Compliant with VESA Display Stream Compression (DSC) 1.1/1.2a
- Two independent DSC video decoders
- 1/2 slices per DSC decoder
- Max resolution width of 4K
- 8/10/12bpc uncompressed data

1.2.6 Pixel Processor

- Support 444-422-420 Color Space Converter
- Support 12-10-8bits Dithering
- Support Down Scaler from 4K to 1080P
- Support SST Output Copy Modes

1.2.7 System Features

- Embedded internal MCU
- Embedded internal Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 DP SST to HDMI Conversion

Based on the DisplayPort SST input and output requirement, GSV2221 can dynamically switch HDMI lane rate in TMDS mode for the best compatibility in 4K/2K timings.

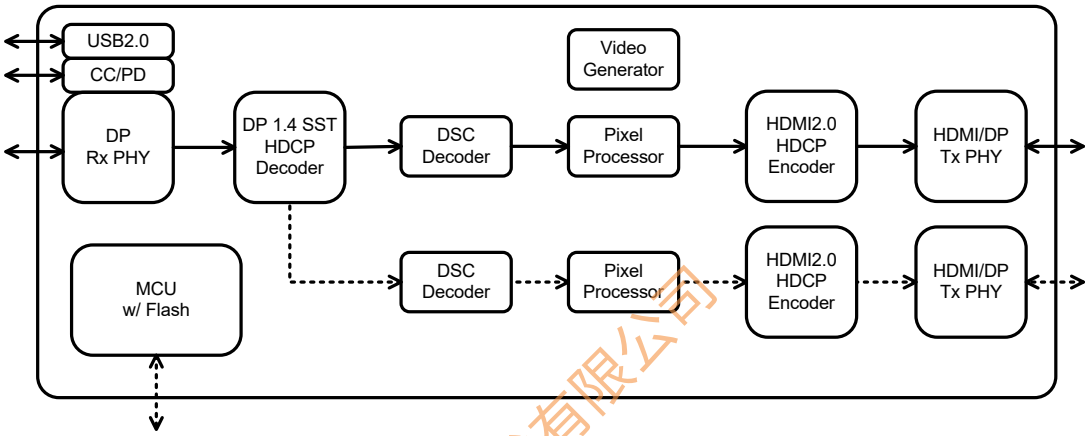


Figure 2. DP SST to HDMI Conversion

1.3.2 DP MST (uncompressed streams) to HDMI Conversion

Based on the DisplayPort MST (more than 2 uncompressed streams) input and output requirement, GSV2221 can dynamically select stream data for the two HDMI TX ports with bypass through DSC decoder.

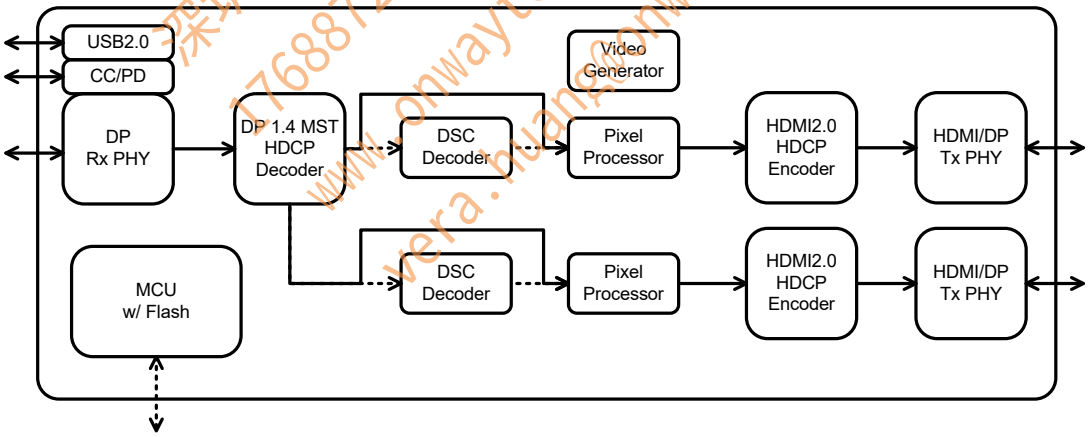


Figure 3. DP MST (uncompressed streams) to HDMI Conversion

1.3.3 DP MST (compressed streams) to HDMI Conversion

Based on the DisplayPort MST (more than 2 compressed streams) input and output requirement, GSV2221 can dynamically select stream data for the two HDMI TX ports with DSC decoder.

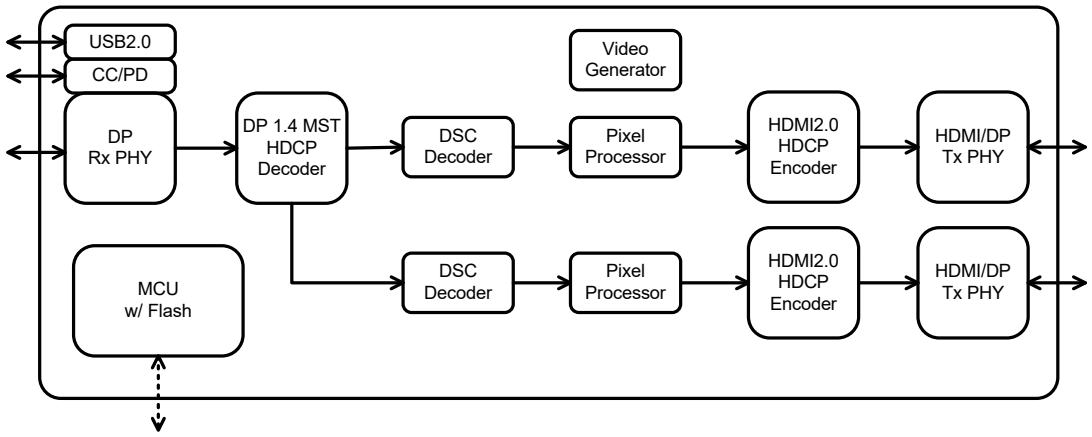


Figure 4. DP MST (compressed streams) to HDMI Conversion

1.3.4 DP SST to DP/eDP Conversion

Based on the DisplayPort SST input and output requirement, GSV2221 can dynamically switch DP/eDP lane rate in DisplayPort mode for the best compatibility in 4K/2K timings.

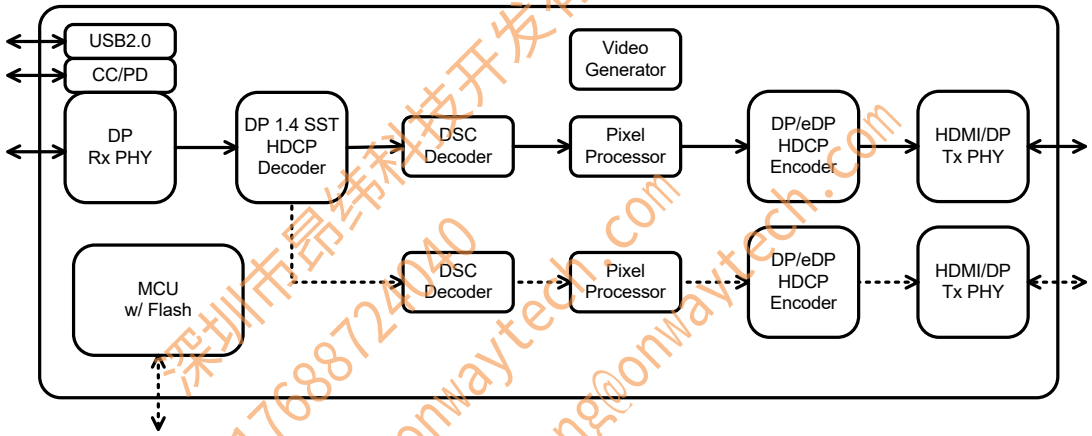


Figure 5. DP SST to DP/eDP Conversion

1.3.5 DP MST (uncompressed streams) to DP/eDP Conversion

Based on the DisplayPort MST (more than 2 uncompressed streams) input and output requirement, GSV2221 can dynamically select stream data for the two DP/eDP TX ports with bypass through DSC decoder.

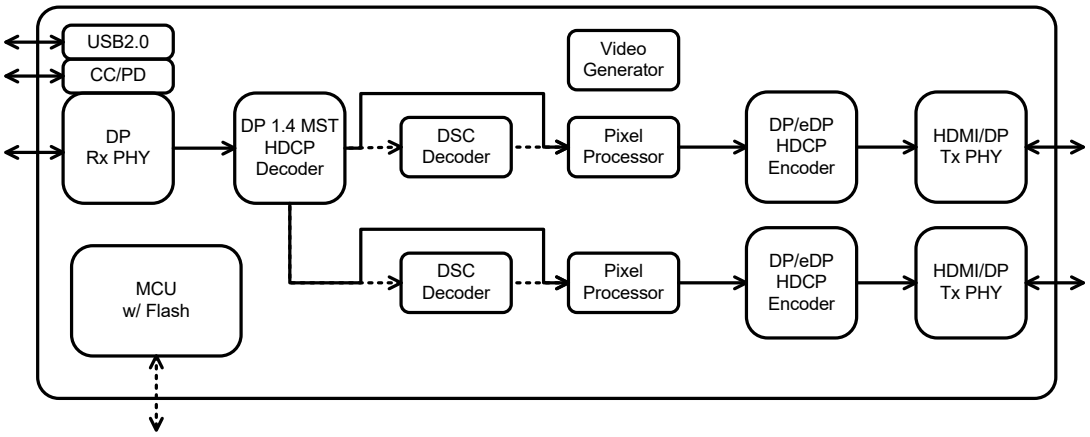


Figure 6. DP MST (uncompressed streams) to DP/eDP Conversion

1.3.6 DP MST (compressed streams) to DP/eDP Conversion

Based on the DisplayPort MST (more than 2 compressed streams) input and output requirement, GSV2221 can dynamically select stream data for the two DP/eDP TX ports with DSC decoder.

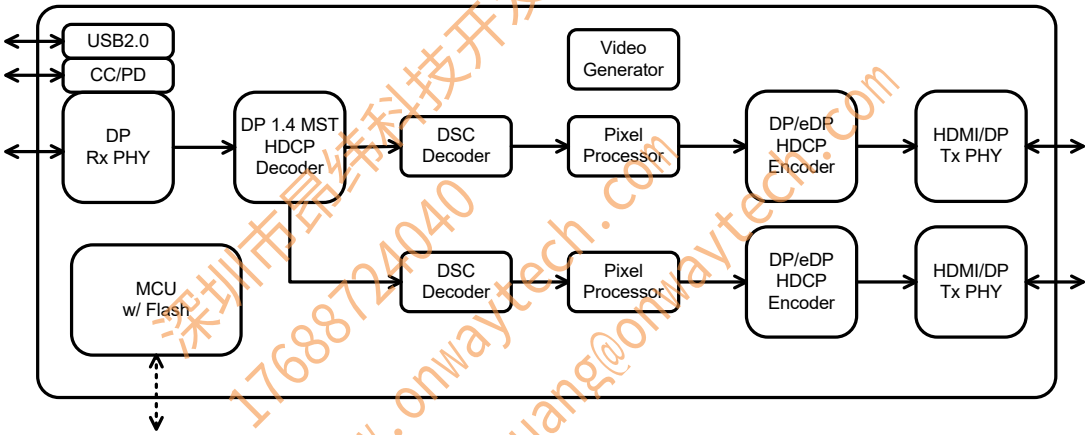


Figure 7. DP MST (compressed streams) to DP/eDP Conversion

2. Pin Description

2.1 Pin Diagram

QFN88 Pin definition is defined as below.

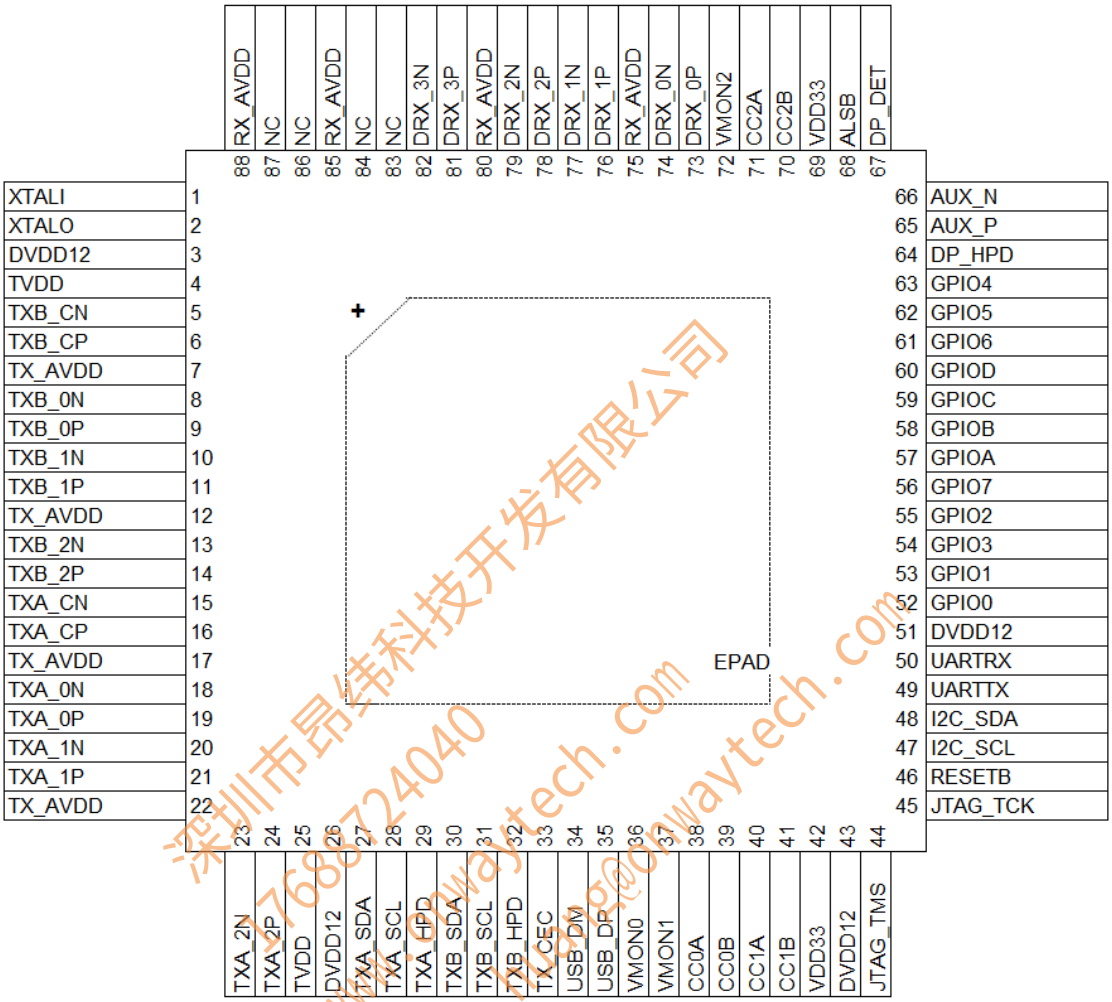


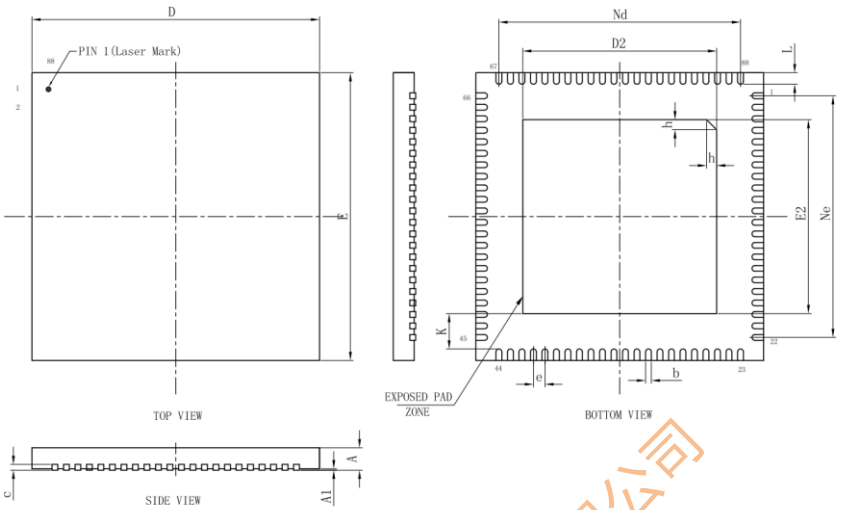
Figure 8. GSV2221 QFN88 Pin Diagram

2.2 Pin Description

Table 2. QFN88 Pin Description

Pin Name	Direction	Pin No.	Description
DisplayPort Rx Pins			
DP_DET	I	67	RX DP Detection PAD
DP_HPD	O	64	RX HPD PAD, can be used as GPIO Input in Type-C Application
AUX_P	I/O	65	RX AUX_P PAD, Type-C SBU_P
AUX_N	I/O	66	RX AUX_N PAD, Type-C SBU_N
DRX_0N	I	74	RX Negative Main-Link differential data input [0]

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	9.90	10.00	10.10
D2	6.64	6.74	6.84
e	0.40BSC		
Nd	8.40REF		
E	9.90	10.00	10.10
E2	6.64	6.74	6.84
Ne	8.40REF		
L	0.30	0.40	0.50
K	0.20	-	-
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	300x300		

Figure 12. Package Dimensions (QFN88)

5. Ordering Guide

Table 6. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV2221	−20°C to +85°C	QFN88	Tray